

CB-1 SWG LOGIC SCHEMATICS

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83.DC/DC VCCGFXCORE_D (TPS51728)
84.BLANK
85.DC/DC VCC1R05AMT(VT356)
86.DC/DC VCC1R35A(VT357)
87.DC/DC VCC0R675B(TPS51200)
88.DC/DC VCC1R5VIDEO(VT356)
89.DC/DC VCC1R05VIDEO_PLL(BD3551HFN)
90.DC/DC VCC1R8B(BD9139)
91.BLANK
92.DC/DC VCC1R5B(BD3551HFN)
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94.LOAD SW LAN
95.LOAD SW VIDEO
96.LOAD SW B
97.BLANK
98.LOAD SW WWAN & WLAN
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100.3rd USB

EC Modify History

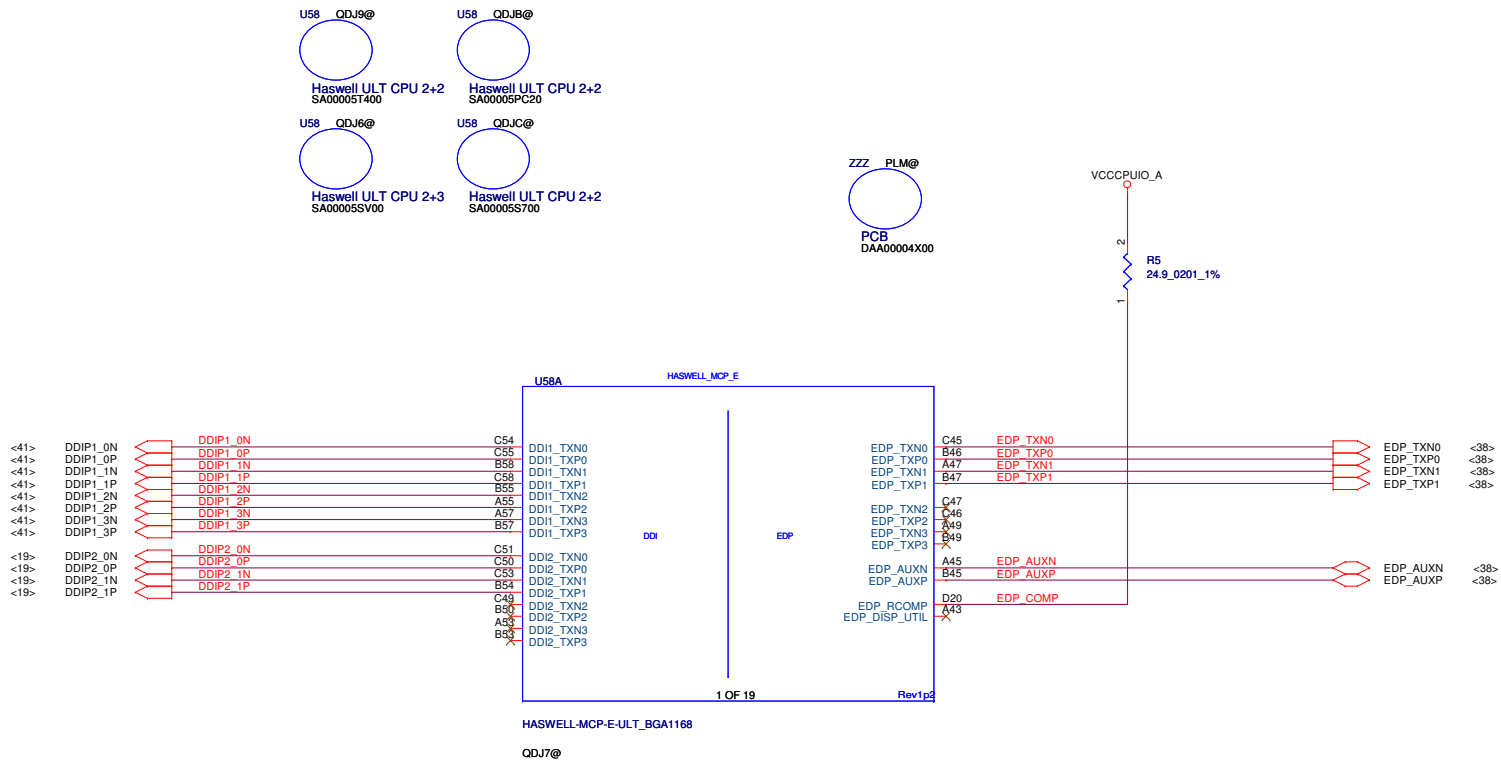
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2013/05/09	JVCB-1_SWG_SIT-SWG_ECR003	JV_CB-1_SWG_SIT_SCH_EC001-005_050901.pdf
2013/05/10	JVCB-1_SWG_SIT-SWG_ECR004	JV_CB-1_SWG_SIT_SCH_EC001-005_051001.pdf
2013/05/14	JVCB-1_SWG_SIT-SWG_ECR005	JV_CB-1_SWG_SIT_SCH_EC001-005_051401.pdf
2013/05/14	JVCB-1_SWG_SIT-SWG_EC006	JV_CB-1_SWG_SIT_SCH_EC001-006_051402.pdf
2013/07/03	JV_CB-1_SWG_SVT_SCH_EC001-004	JV_CB-1_SWG_SVT_SCH_EC001-004_070301.pdf

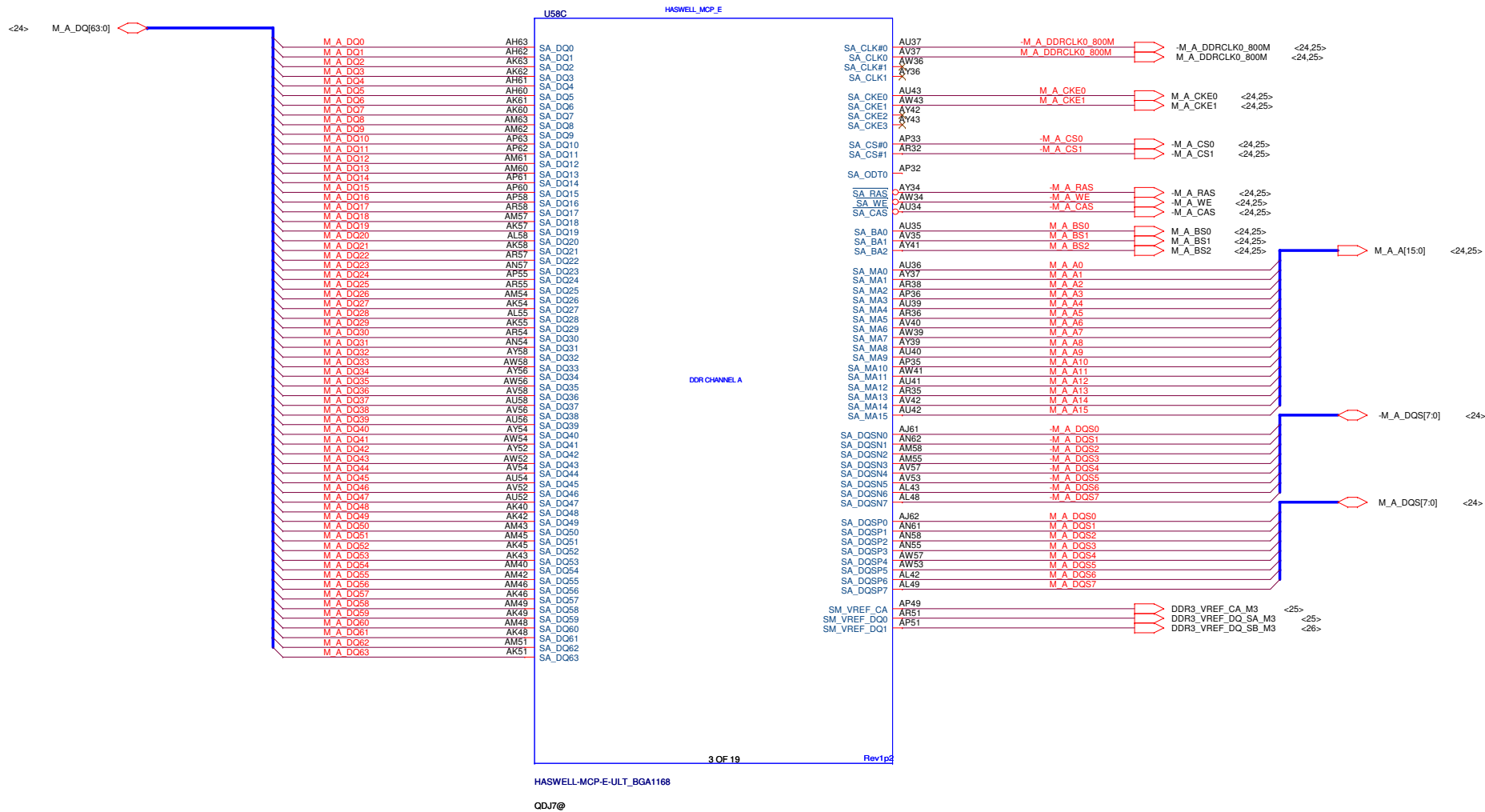
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2012/10/09	CB_1_SWG_SDV_EC011	JV_CB-1_SWG_SDV1_SCH_EC009-010_100801.pdf
2012/10/12	CB_1_SWG_SDV_EC012	JV_CB-1_SWG_SDV1_SCH_EC010-011_101101.pdf
2012/10/13	CB_1_SWG_SDV_EC013	JV_CB-1_SWG_SDV1_SCH_EC011-012_101201.pdf
2012/10/16	CB_1_SWG_SDV_EC014	JV_CB-1_SWG_SDV1_SCH_EC013_101501.pdf
2012/10/17	CB_1_SWG_SDV_EC015	JV_CB-1_SWG_SDV1_SCH_EC014_101601.pdf
2012/10/18	CB_1_SWG_SDV_EC016	JV_CB-1_SWG_SDV1_SCH_EC015_101701.pdf
2012/10/19	CB_1_SWG_SDV_EC017	JV_CB-1_SWG_SDV1_SCH_EC016_101801.pdf
2012/10/20	CB_1_SWG_SDV_EC018	JV_CB-1_SWG_SDV1_SCH_EC017_101901.pdf
2012/10/25	CB_1_SWG_SDV_EC018-022	JV_CB-1_SWG_SDV1_SCH_EC018-021_102401.pdf
2012/10/31	CB_1_SWG_SDV_EC023	JV_CB-1_SWG_SDV1_SCH_EC022_103001.pdf
2012/10/32	CB_1_SWG_SDV_EC023-025	JV_CB-1_SWG_SDV1_SCH_EC023-024_103101.pdf
2012/11/15	CB_1_SWG_SDV_EC025-033	JV_CB-1_SWG_SDV1_SCH_EC025-032_111401.pdf
2012/11/23	CB_1_SWG_SDV_EC033-036	JV_CB-1_SWG_SDV1_SCH_EC025-035_112201.pdf
2012/11/27	CB_1_SWG_SDV_EC037	JV_CB-1_SWG_SDV1_SCH_EC036_112601.pdf
2012/12/05	CB_1_SWG_SDV_EC037-039	JV_CB-1_SWG_SDV_SCH_EC037-038_120401.pdf

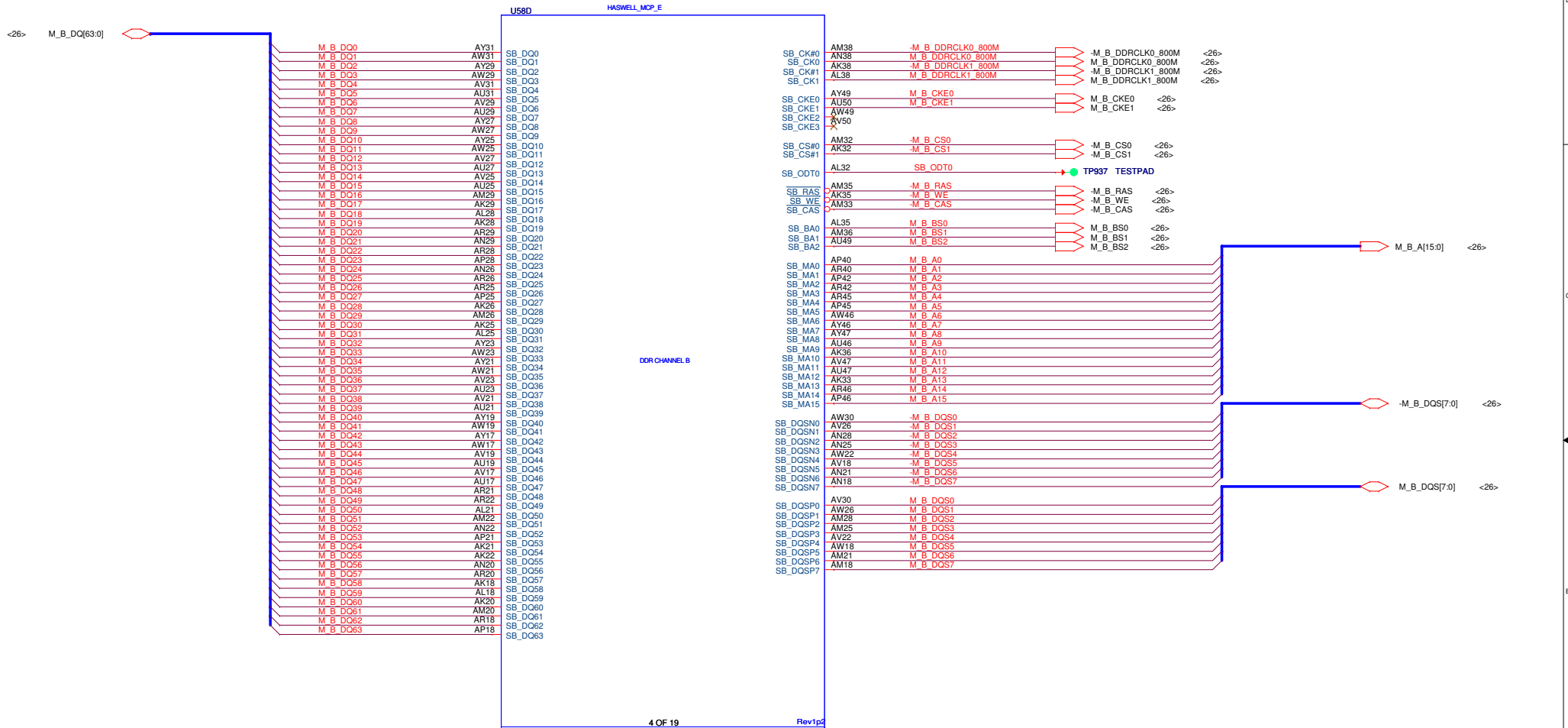
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COBAIN SWG





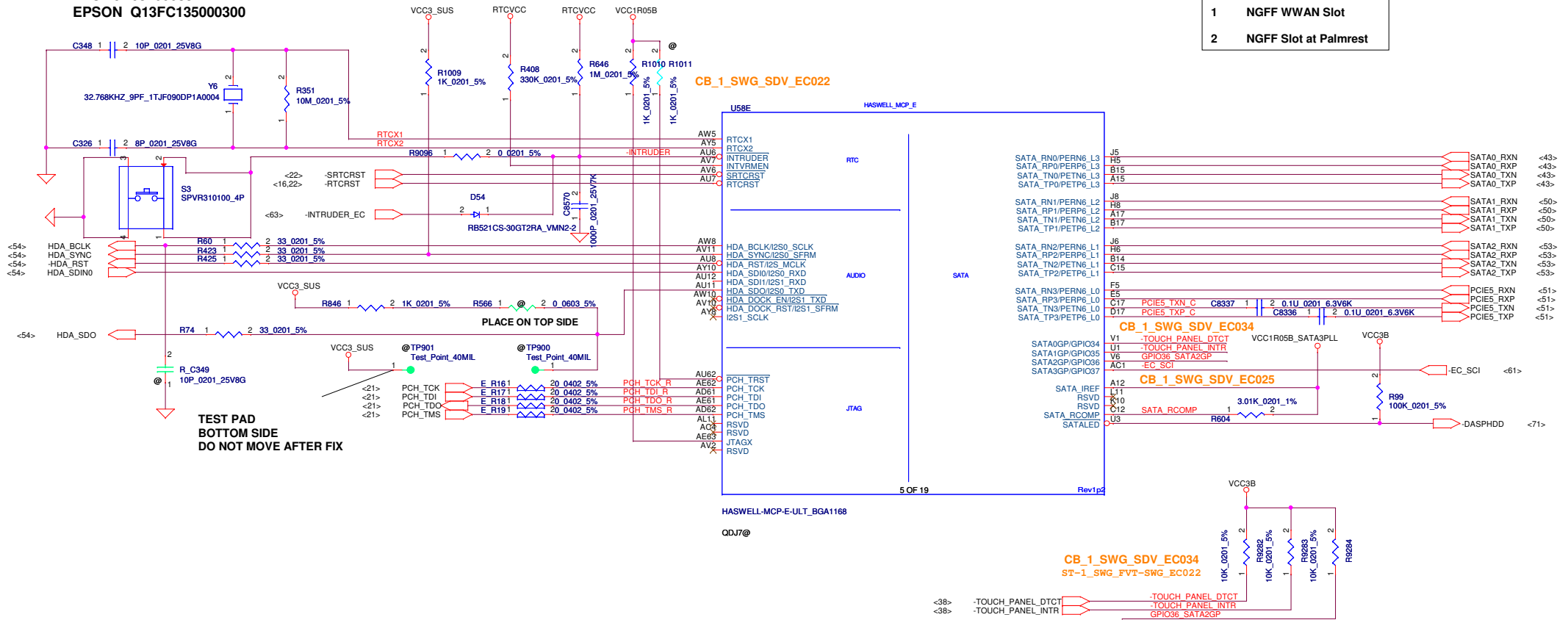


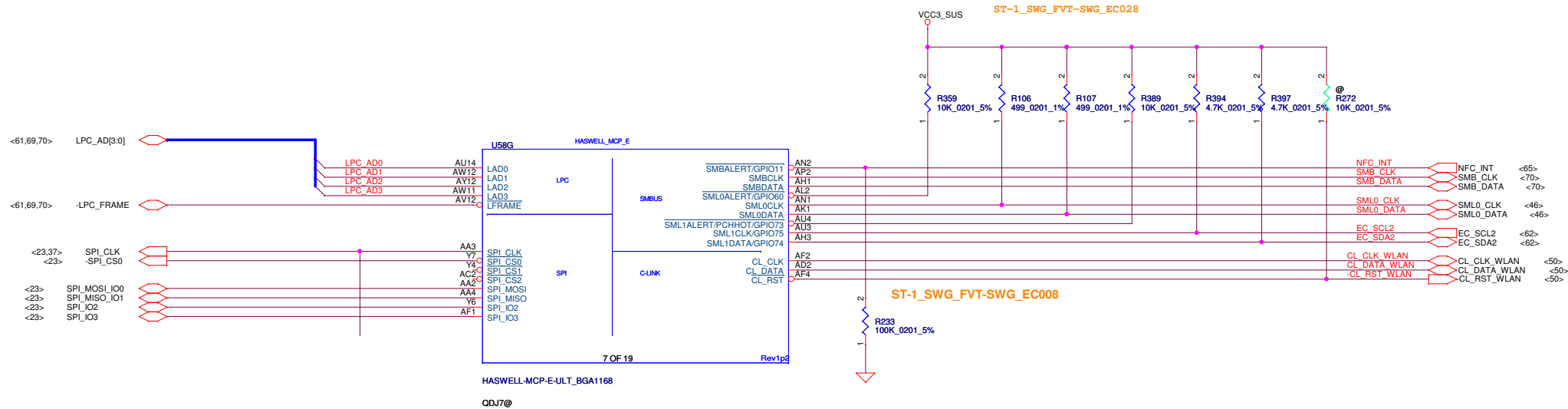
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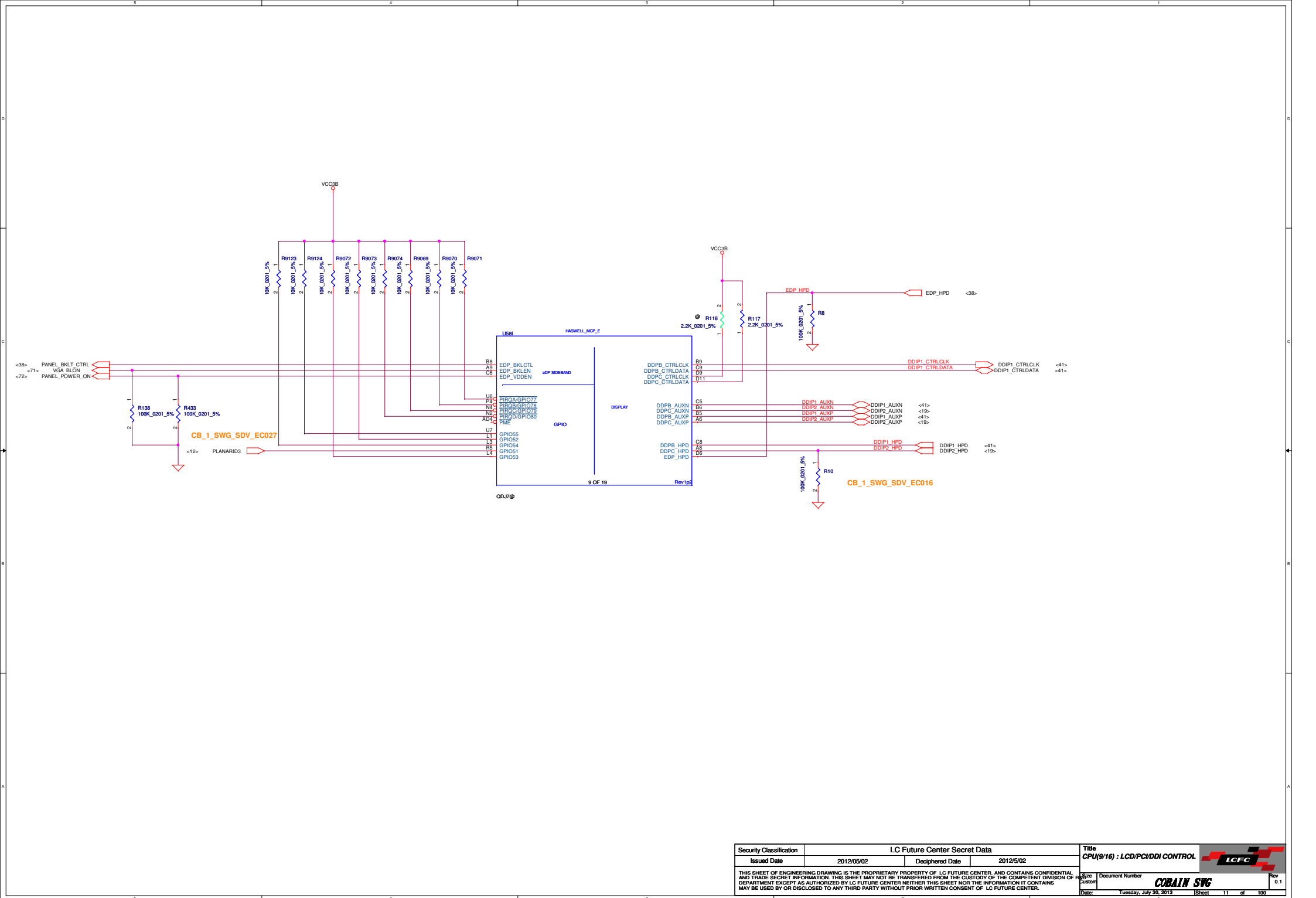
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EPSON Q13FC135000300

SATA Port Assignment	
0	HDD Connector
1	NGFF WWAN Slot
2	NGFF Slot at Palmrest





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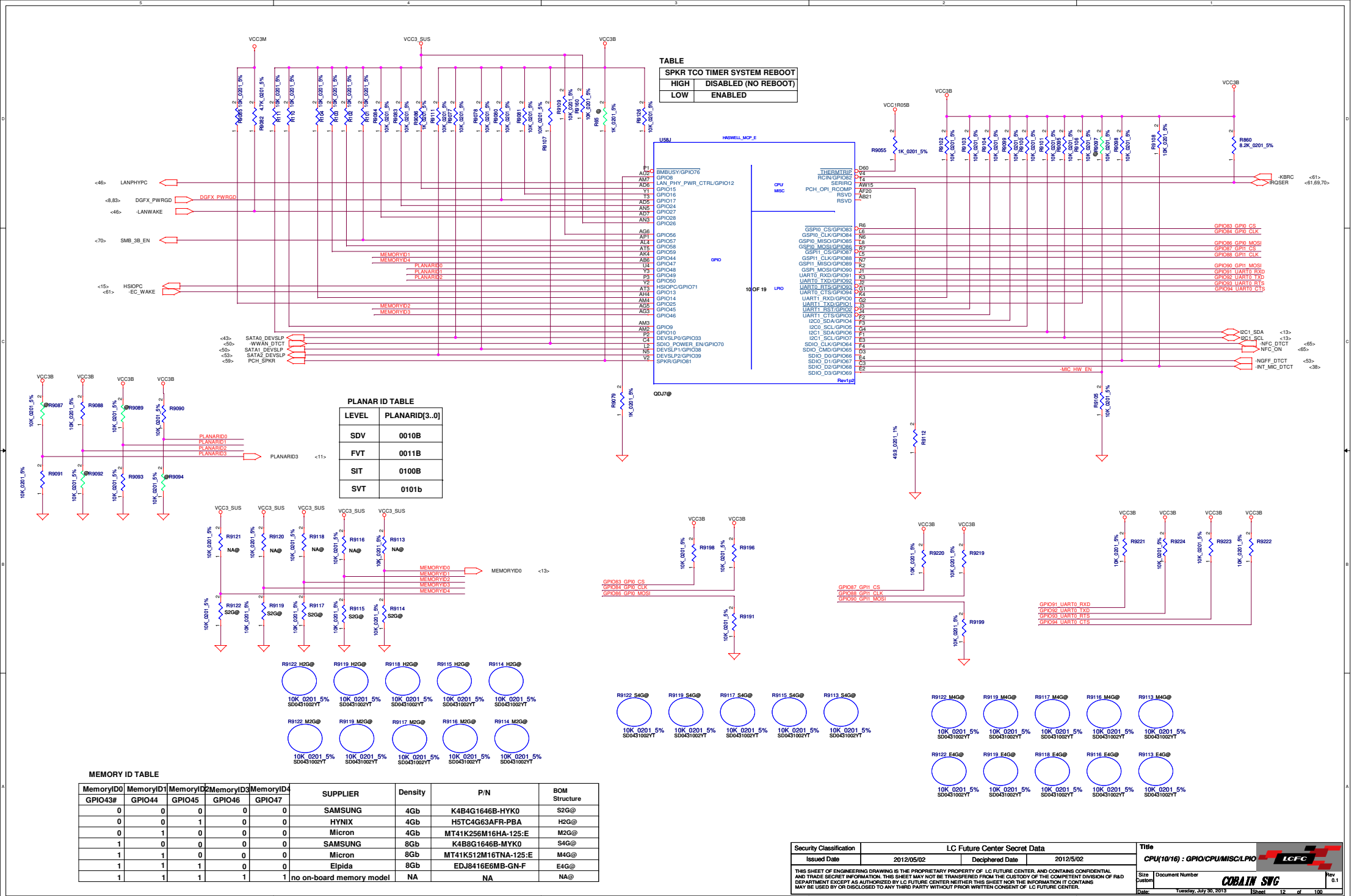



TABLE	
SPKR TCO TIMER SYSTEM REBOOT	
HIGH	DISABLED (NO REBOOT)
LOW	ENABLED

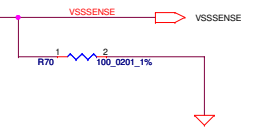
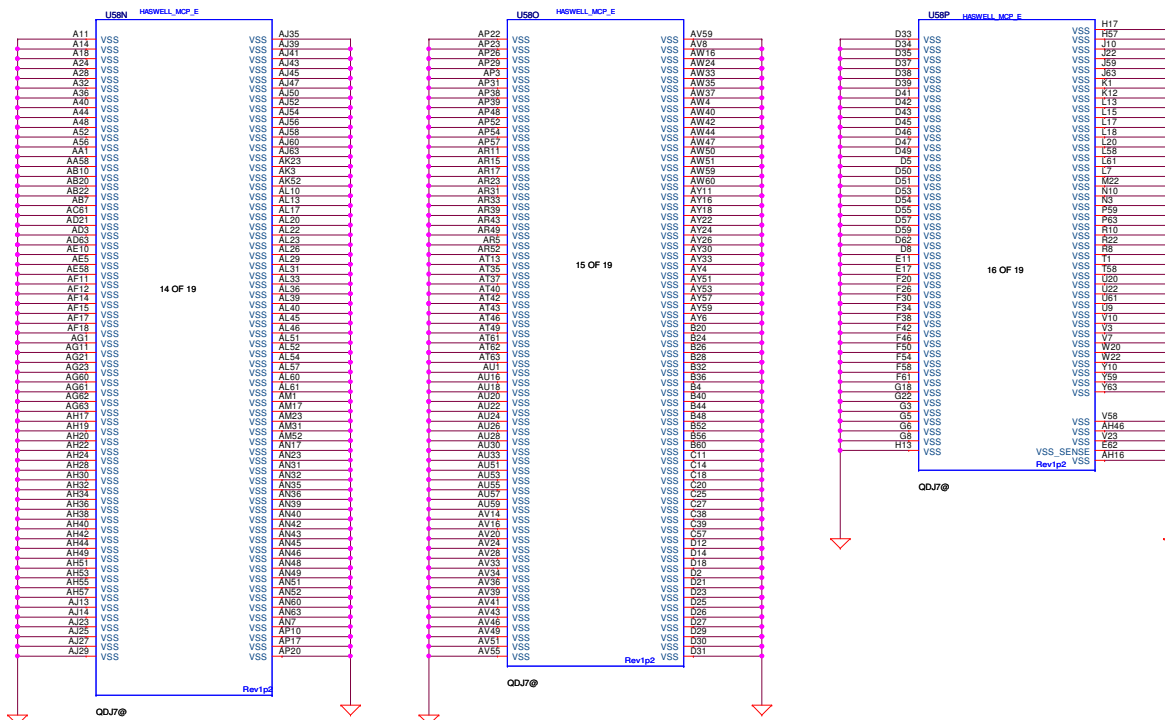
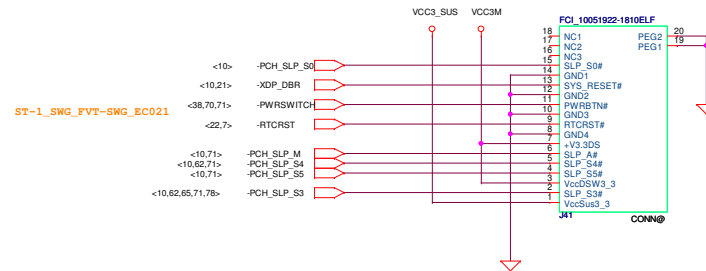
PLANAR ID TABLE	
LEVEL	PLANARID[3..0]
SDV	0010B
FVT	0011B
SIT	0100B
SVT	0101b


MEMORY ID TABLE

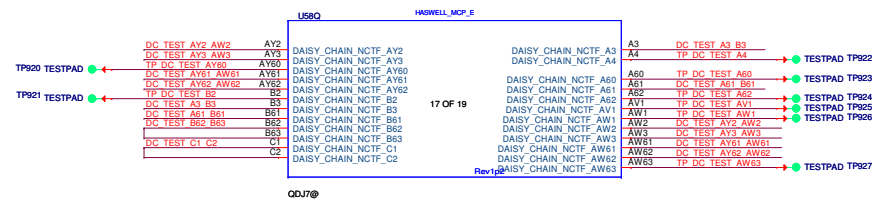
MemoryID0	MemoryID1	MemoryID2	MemoryID3	MemoryID4	SUPPLIER	Density	P/N	BOM Structure
GPIO43#	GPIO44	GPIO45	GPIO46	GPIO47				
0	0	0	0	0	SAMSUNG	4Gb	K4B4G1646B-HYK0	S2G@
0	0	1	0	0	HYNIX	4Gb	H5TC4G63AFR-PBA	H2G@
0	1	0	0	0	Micron	4Gb	MT41K256M16HA-125:E	M2G@
1	0	0	0	0	SAMSUNG	8Gb	K4B8G1646B-MYK0	S4G@
1	1	0	0	0	Micron	8Gb	MT41K512M16TNA-125:E	M4G@
1	1	1	0	0	Elpida	8Gb	EDJ8416E6MB-GN-F	E4G@
1	1	1	1	1	no on-board memory model	NA	NA	NA@



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		COBAIN SVC	
		Rev 0.1	

APS/PETS Interface

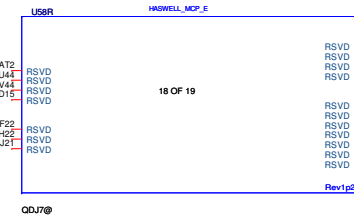



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CFG4: Display Port Presence
1: Disabled 0: Enabled



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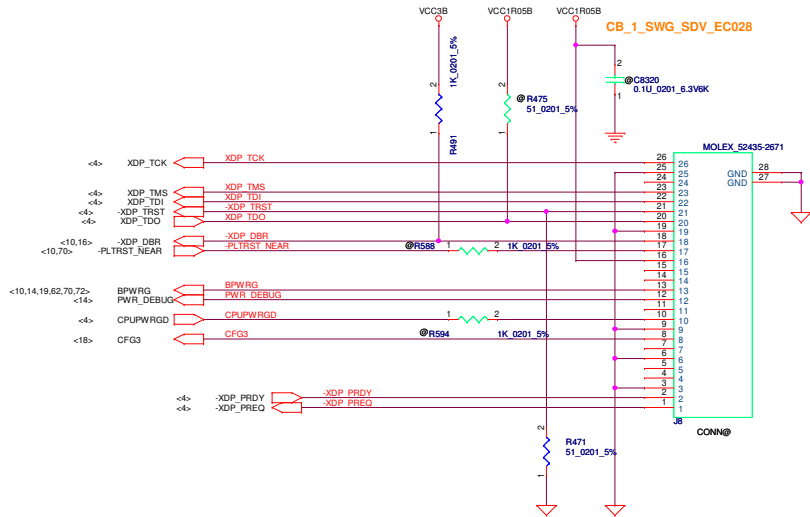


TABLE NOTE: J8 "ASM" FOR PDV/SDV ONLY.

SIGNAL	REF DES	ENABLE	DISABLE
TDO	R475	ASM	NO ASM
TRST#	R471	ASM	ASM
DBRST#	R491	ASM	ASM
RESET#	R588	ASM	NO ASM
PWRGD	R594	ASM	NO ASM
	J8	ASM	NO ASM

↑
LOGIC

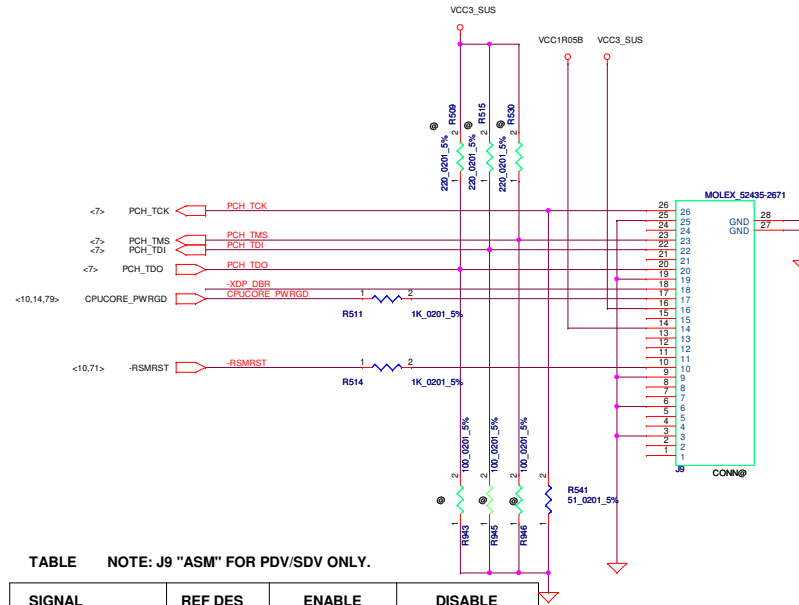
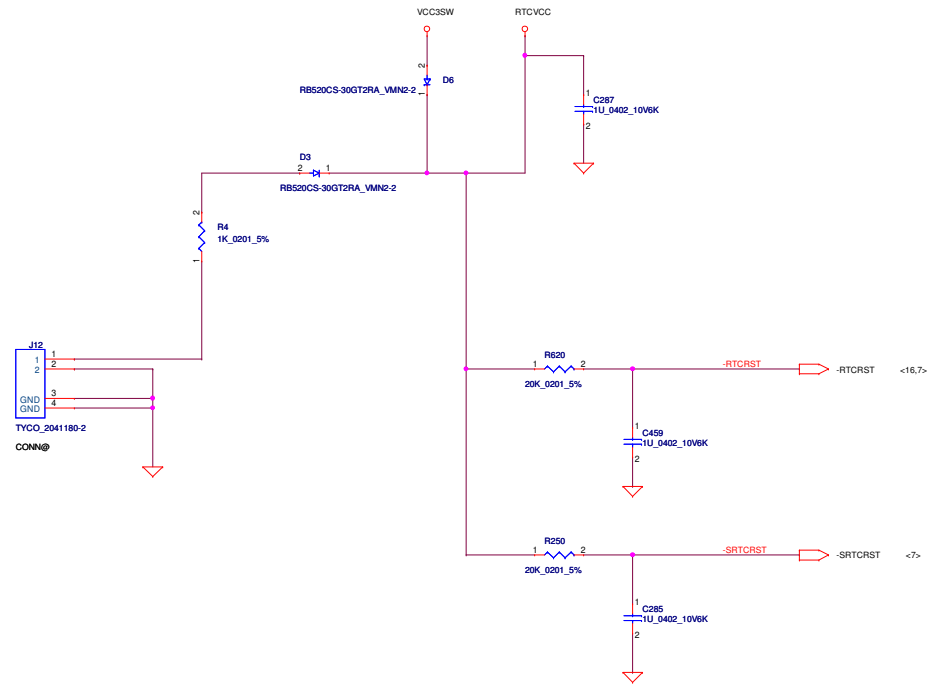



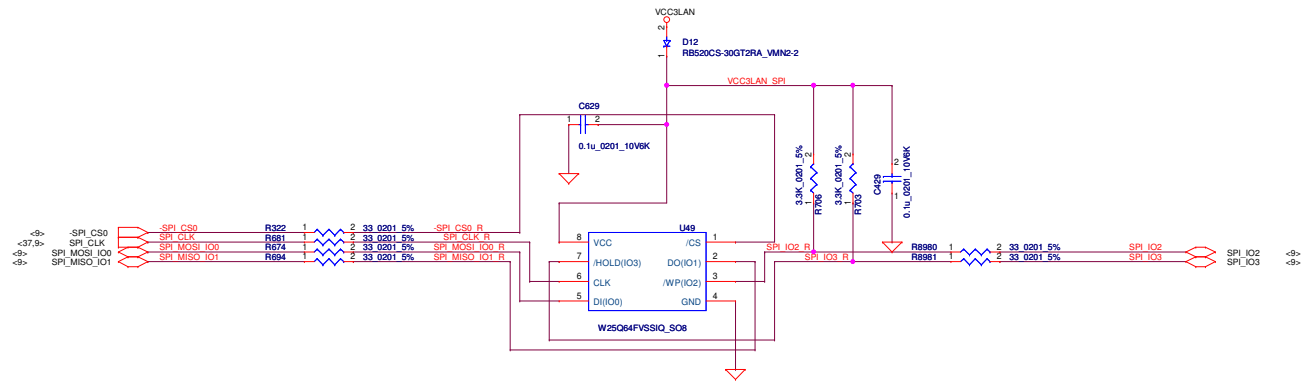
TABLE NOTE: J9 "ASM" FOR PDV/SDV ONLY.

SIGNAL	REF DES	ENABLE	DISABLE
TDO	R509 R943	220 100	NO ASM NO ASM
TMS	R530 R946	220 100	NO ASM NO ASM
TDI	R515 R945	220 100	NO ASM NO ASM
TCK	R541	51	51
CPUCORE_PWRGD	R511	ASM	NO ASM
-RSMRST	R514	ASM	NO ASM
	J9	ASM	NO ASM

↑
LOGIC



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Revision		1		Document Number		1870	



TABLE

SF100 PIN HEADER INTERFACE (TOP VIEW)							
1	VCC	D12.1	GND	GND	2		
3	CS#	R322.2	R681.2	CLK	4		
5	MISO	R694.2	R674.2	MOSI	6		
7	(KEY)	N/A	N/A	(RESET)	8		

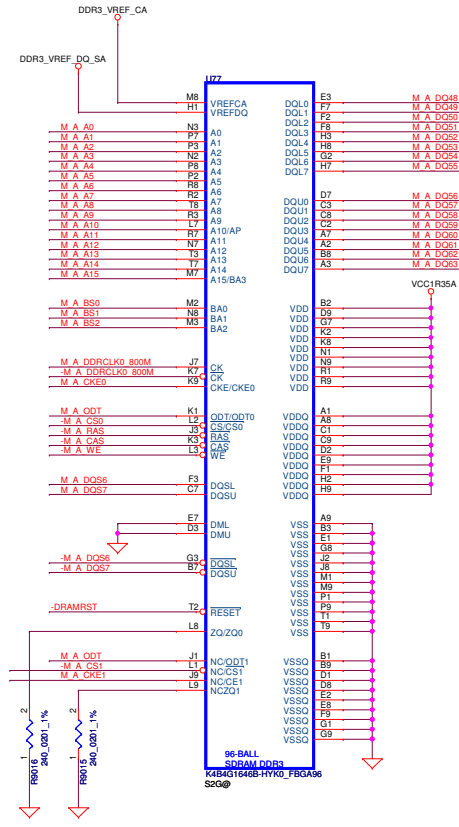
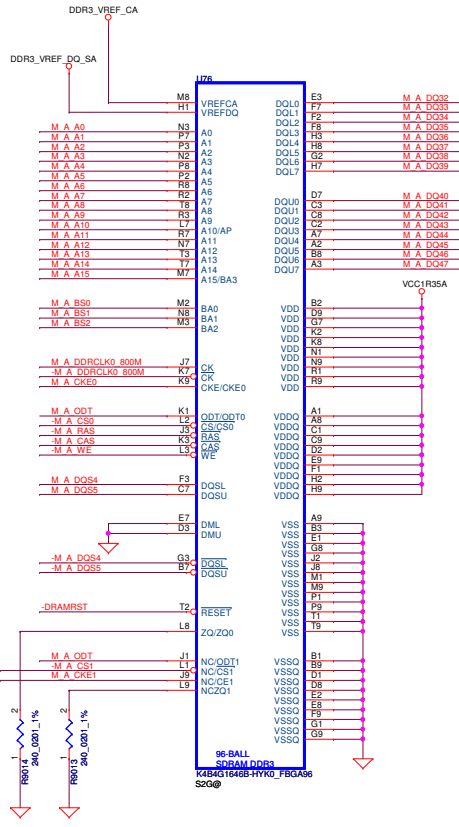
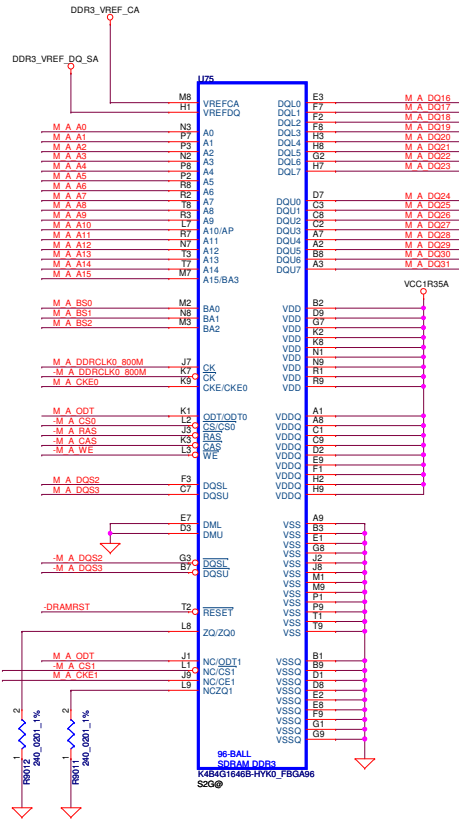
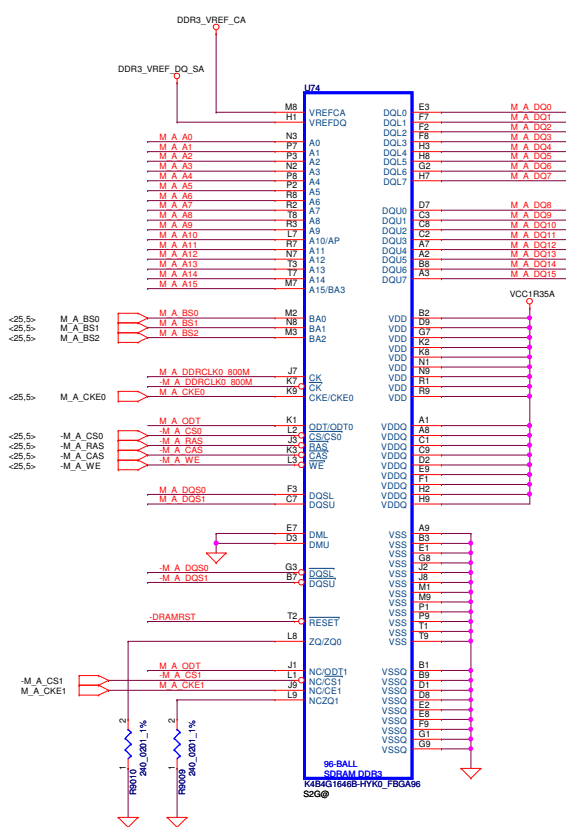
U49 SPI ROM

vPro Model (16MB)		Non-vPro Model (8MB)	
WINBOND	W25Q128FVSIQ	WINBOND	W25Q64FVSSIQ
MACRONIX	MX25L12875FM2I-10G	MACRONIX	MX25L6475EM2I-10G
MICRON	N25Q128A13ESEC0F	MICRON	N25Q064A13ESEC0F

CB-1_SWG_SDV_EC037

ST-1_SWG_FVT-SWG_EC016

<5> M_A_DQ[63:0]
<5> -M_A_DQS[7:0]
<5> M_A_DQS[7:0]
<25.5> M_A_A[15:0]



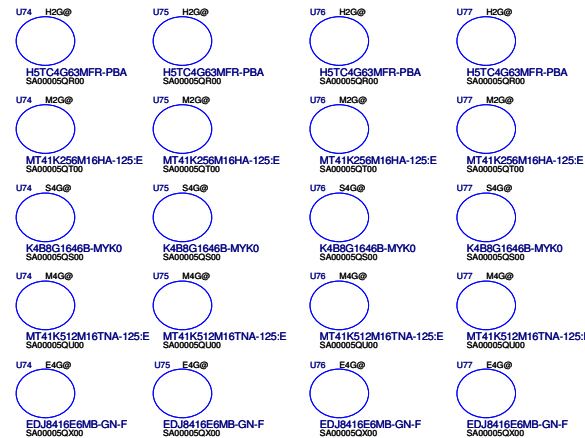
<25.5> M_A_DDRCLK0_800M M_A_DDRCLK0_800M

CB_1_SWG_SDV_EC004

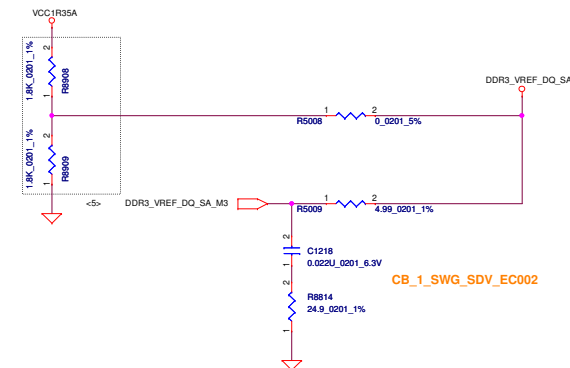
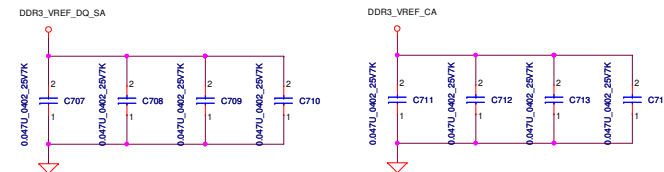
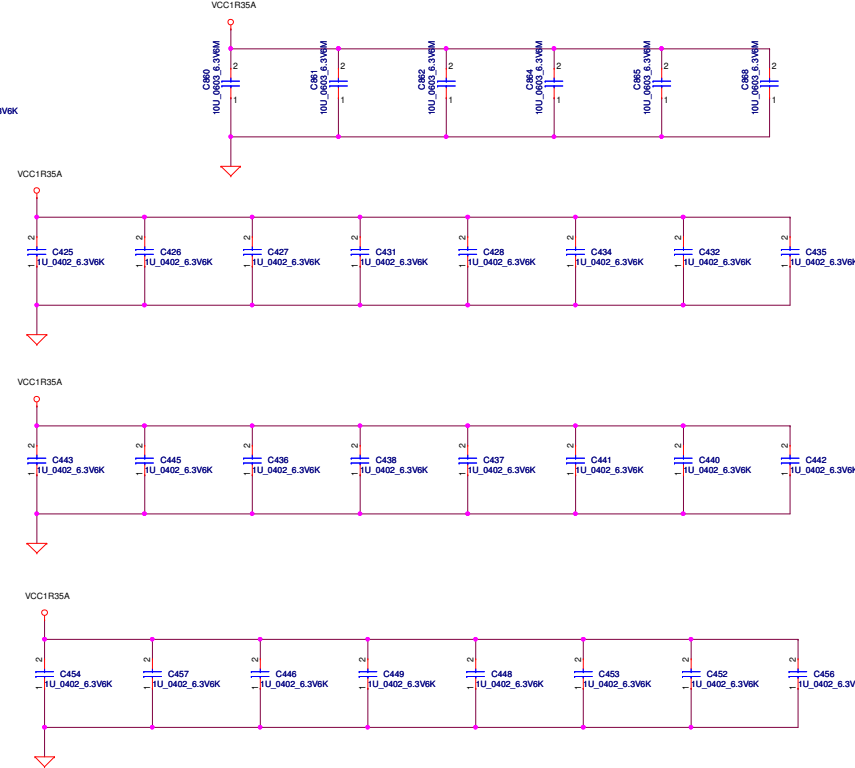
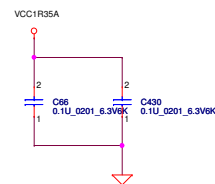
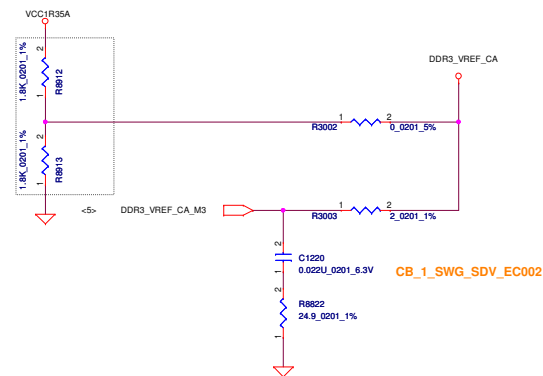
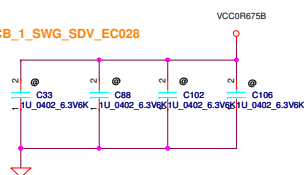
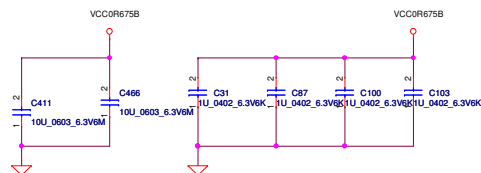
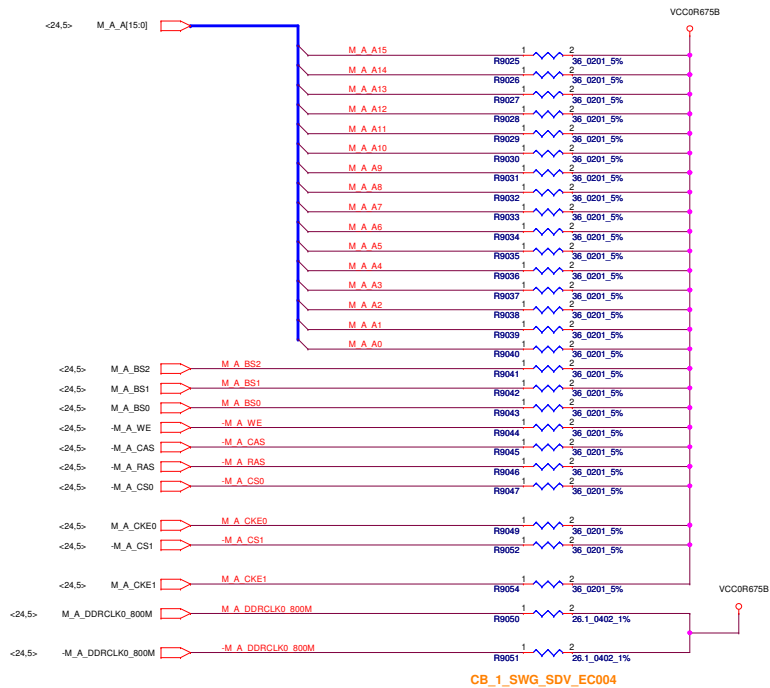
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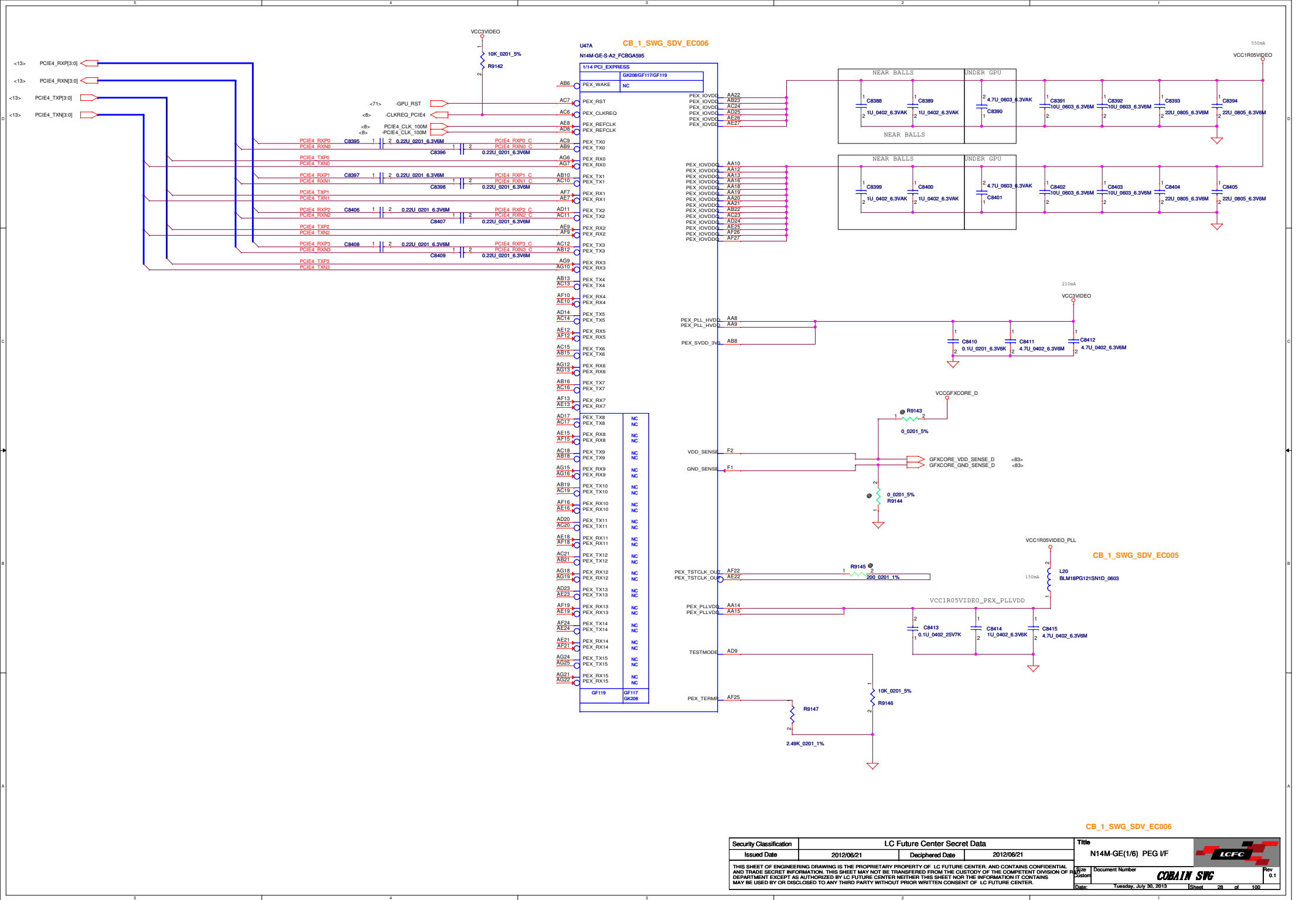
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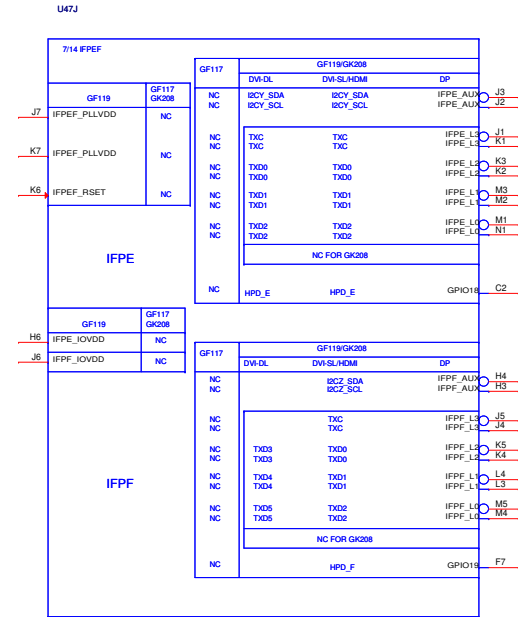
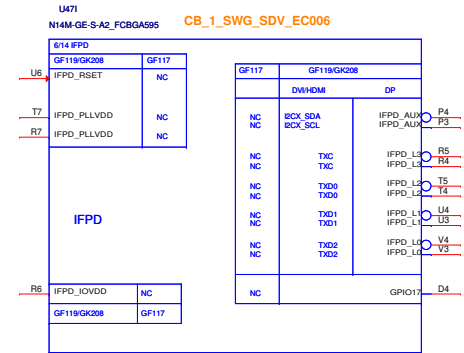
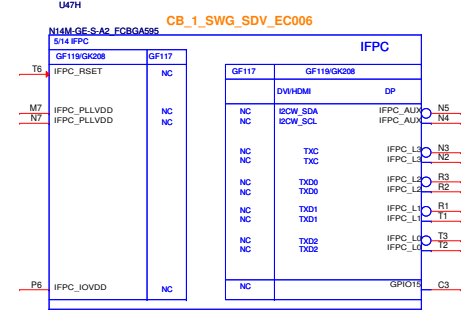
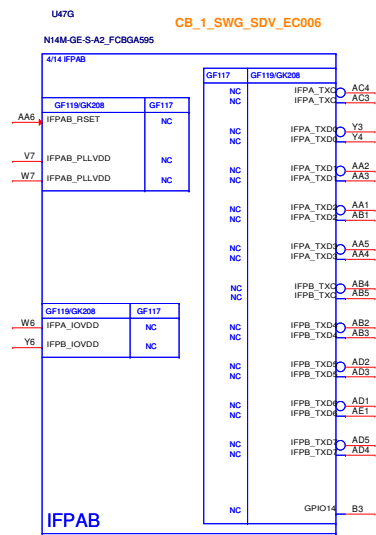
<26.4> -DRAMRST -DRAMRST



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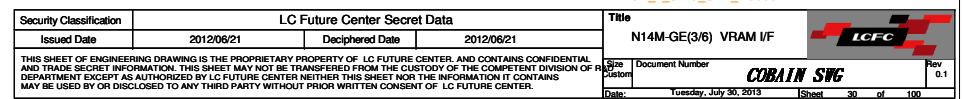


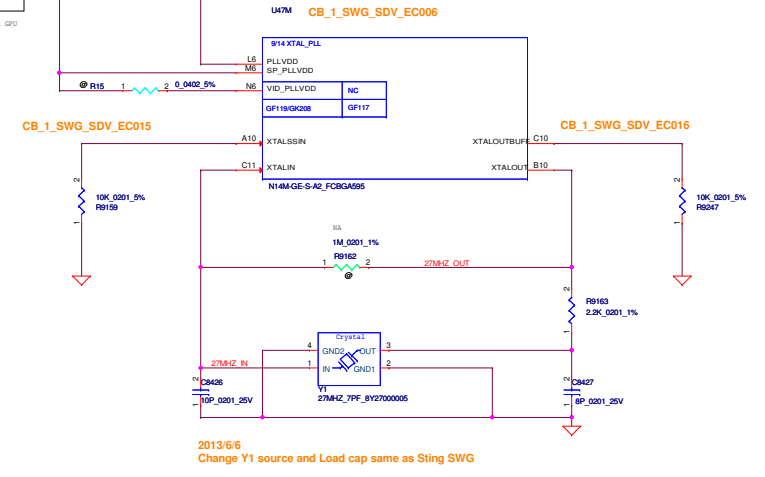
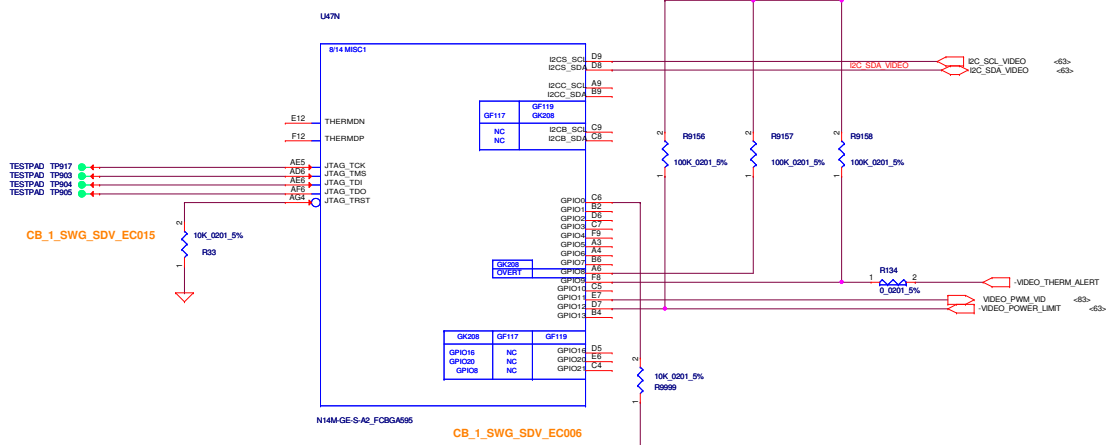
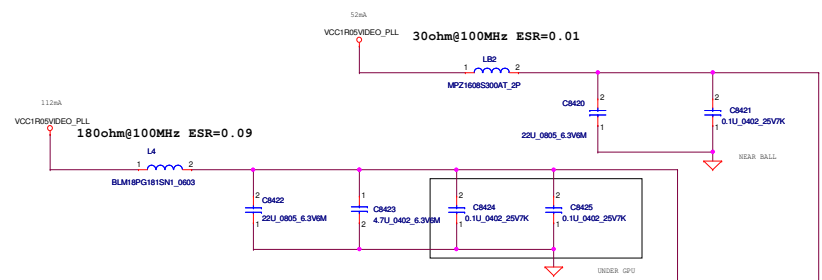
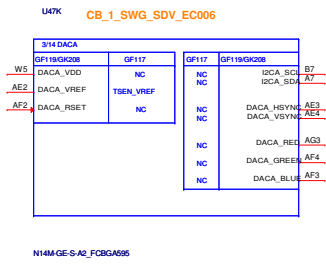




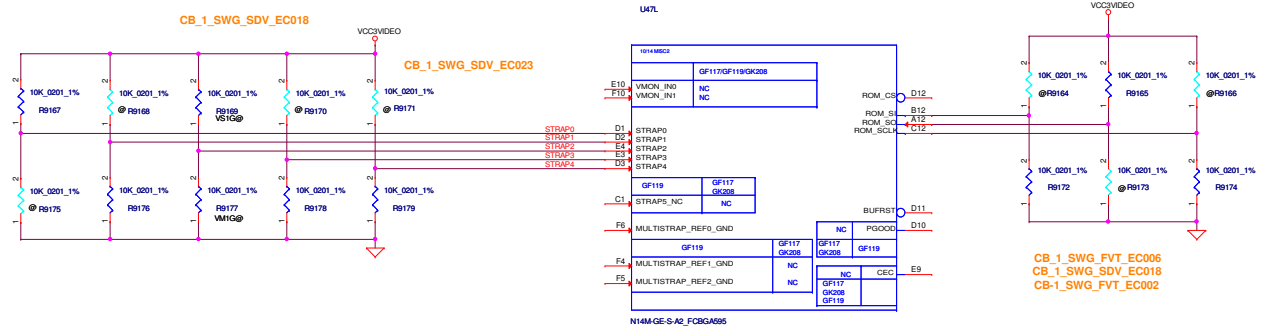
CB_1_SWG_SDV_EC006

N14M-GE-S-A2_FCBGA595





KDS	12ZHA27000CC0A
TXC	8Y27000005
EPSON	Q22FA1280007000



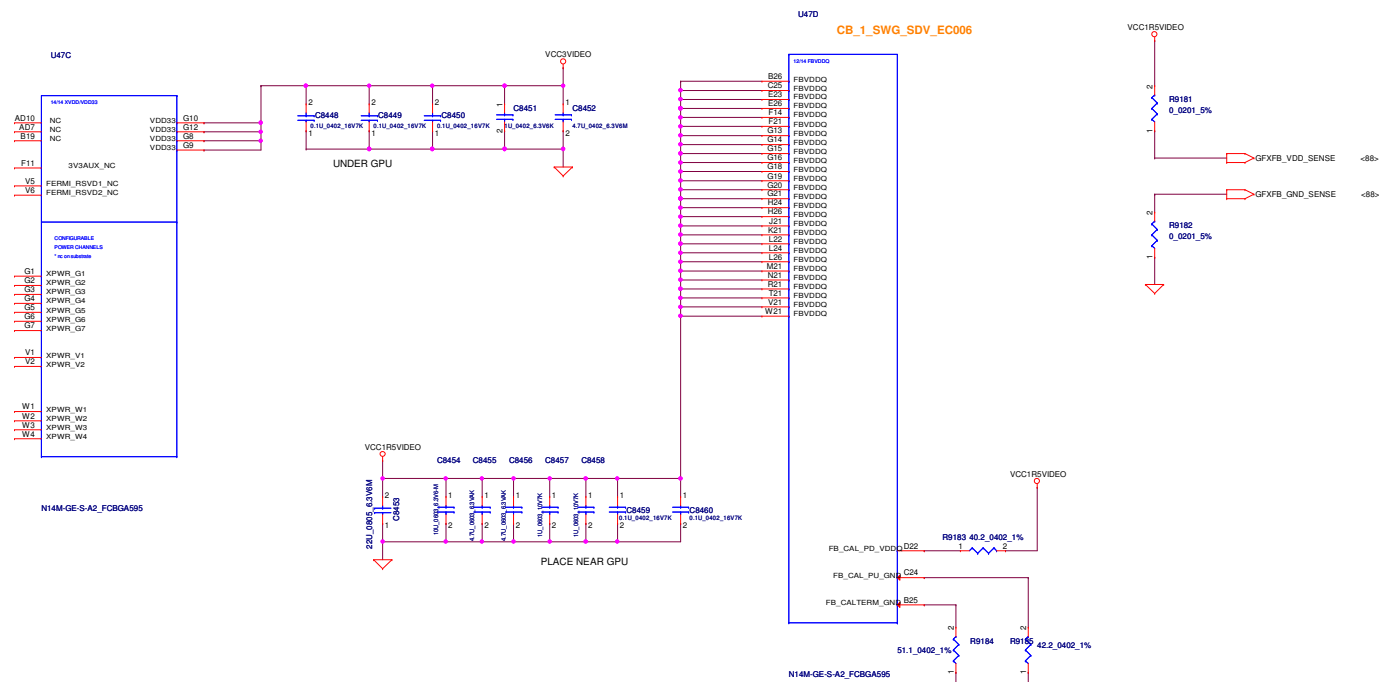
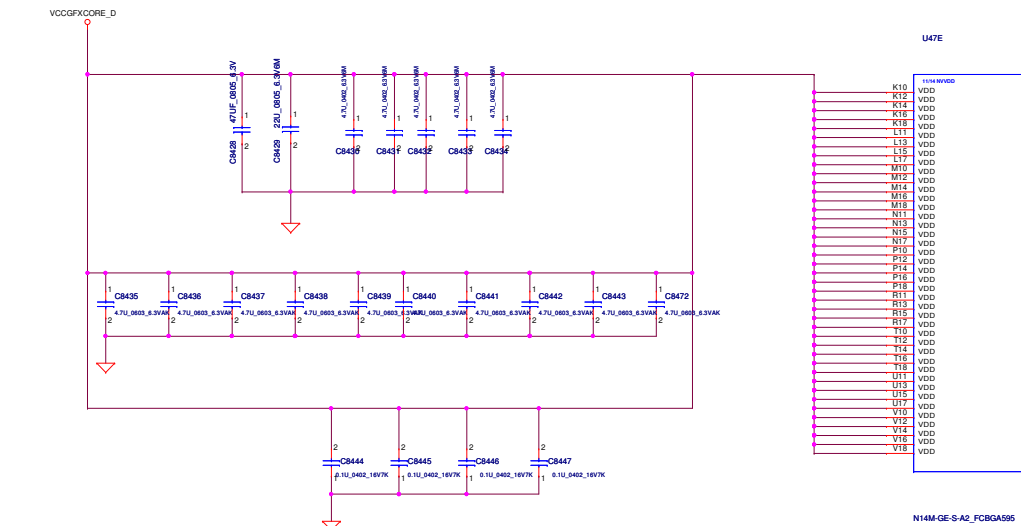
CB_1_SWG_SDV_EC019

Samsung 1GB(K4W2G1646E-BC1A)							
STRAP 0		STRAP 1		STRAP 2		STRAP 3	
R9167	ASM	R9168	No ASM	R9169	ASM	R9170	No ASM
R9175	No ASM	R9176	ASM	R9177	No ASM	R9178	ASM


Micron 1GB(MT41J128M16JT-093G:K)							
STRAP 0		STRAP 1		STRAP 2		STRAP 3	
R9167	ASM	R9168	No ASM	R9169	No ASM	R9170	No ASM
R9175	No ASM	R9176	ASM	R9177	ASM	R9178	ASM

← LOGIC

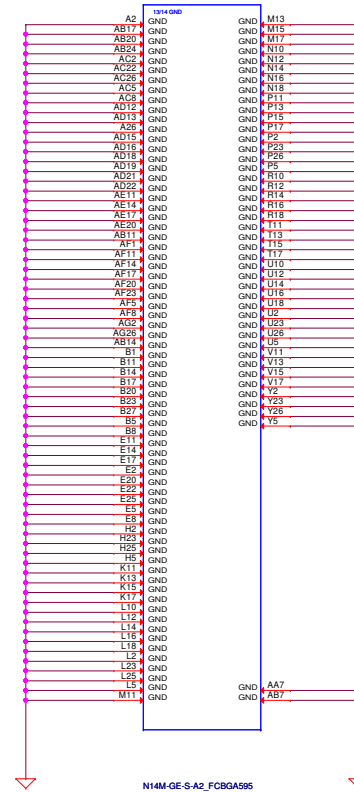
IF N14M-NE1/GE is used, change R9180 from 40.2K to NC



CB_1_SWG_SDV_EC006

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2012/06/21		2012/06/21				
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				Date	Tuesday, July 30, 2013	Sheet
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U47F CB_1_SWG_SDV_EC006



CB_1_SWG_SDV_EC006


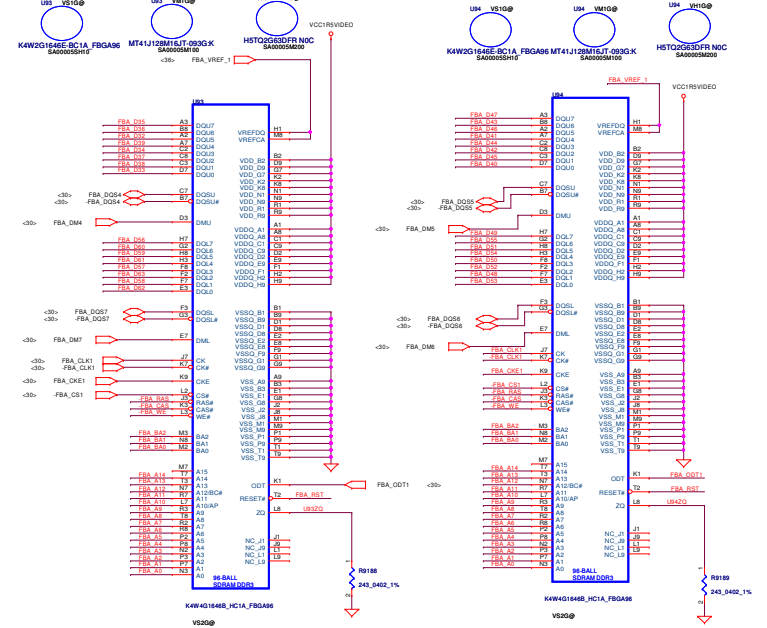
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Issued Date	2012/06/21	Deciphered Date	2012/06/21	N14M-GE(6/6) GND			
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					CORBIN SWG	0.1	
				Date	Tuesday, July 30, 2013	Sheet	33 of 100

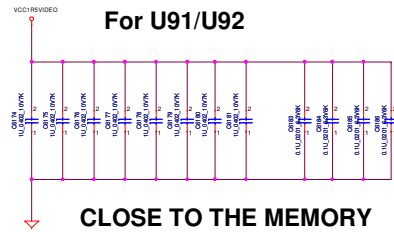
TABLE
DDR3 VIDEO MEMORY

	Micron 2GBITS (128Mx16)	HYNIX 2GBITS(128Mx16)	SAMSUNG 2GBITS(128Mx16)	SAMSUNG 4GBITS(256Mx16)	HYNIX 4GBITS(256Mx16)
U91 U92 U93 U94	MT41J128M16JT-093G-K	HSTQ2G63DFR N0C	K4W201646E-BC1A	K4W4G1646B-HC1A	TBD
BOM Structure	VM1G@	VH1G@	VS1G@	VS2G@	

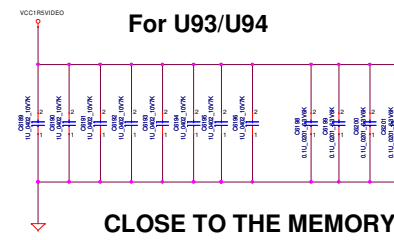
Notification
Sting-1 accepts 1GB support with DDR3. But Sting-1 has potential of 2GB support.
So we should check up 2GB(K4W4G1646B-HC1A) placement. K4W4G1646B-HC1A has largest X axis length (10mm) in VRAM.
MT41J128M16JT-093G-K has largest Y axis length (14mm). So estimation package size is most largest case (10mm * 14mm).





For U91/U92

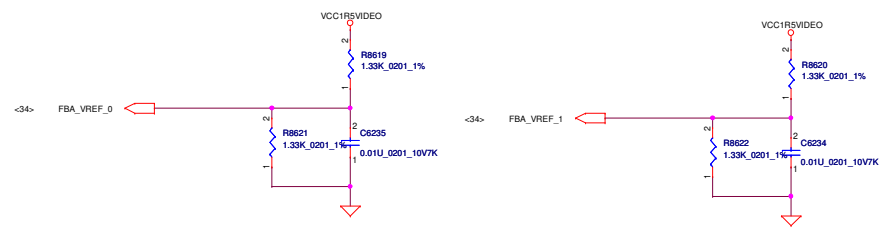


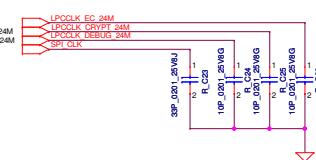
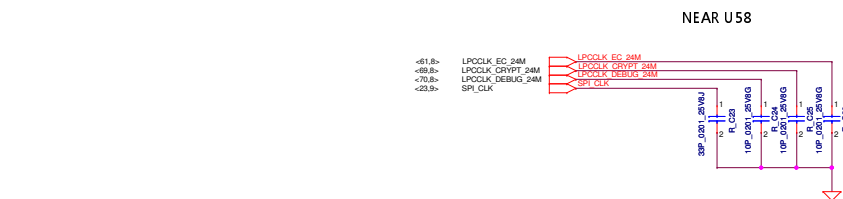
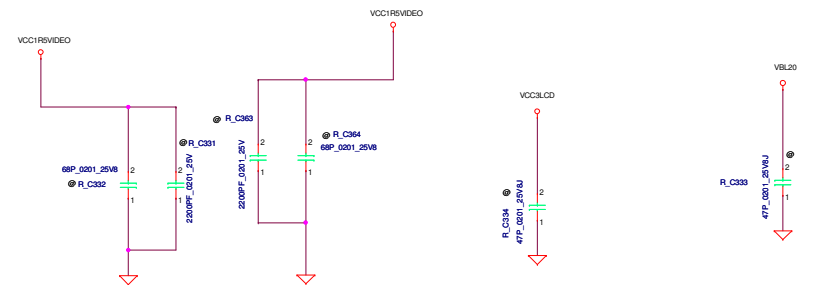
For U93/U94



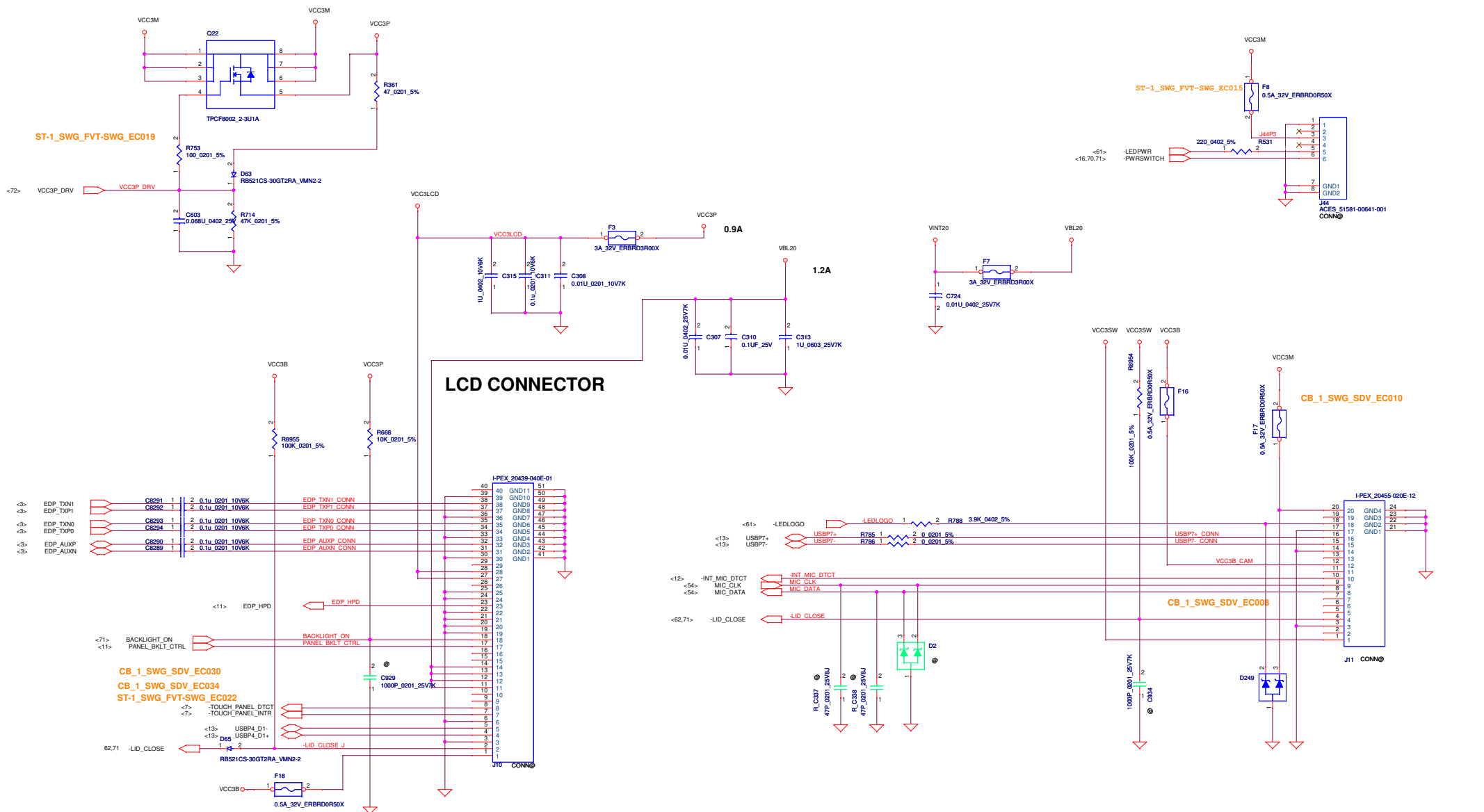
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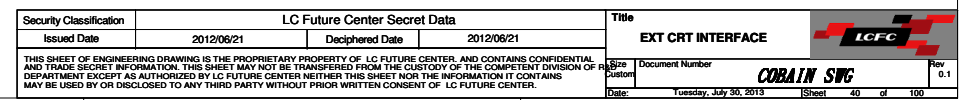
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				Sheet	37 of 100

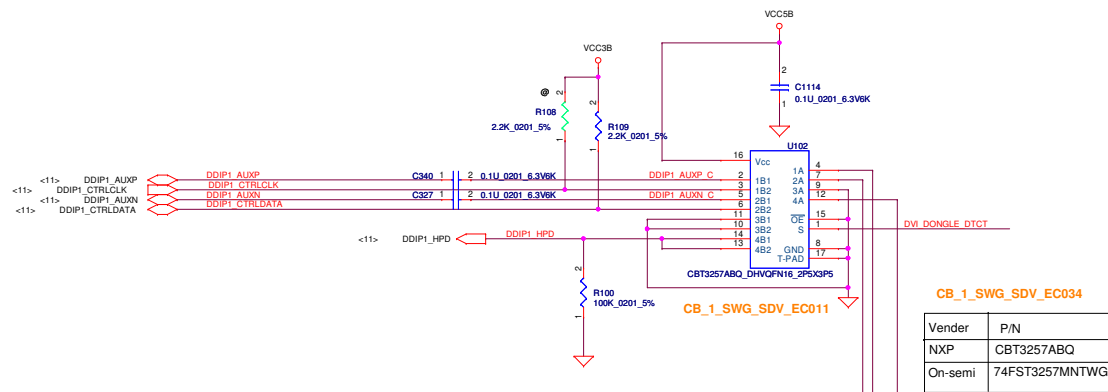


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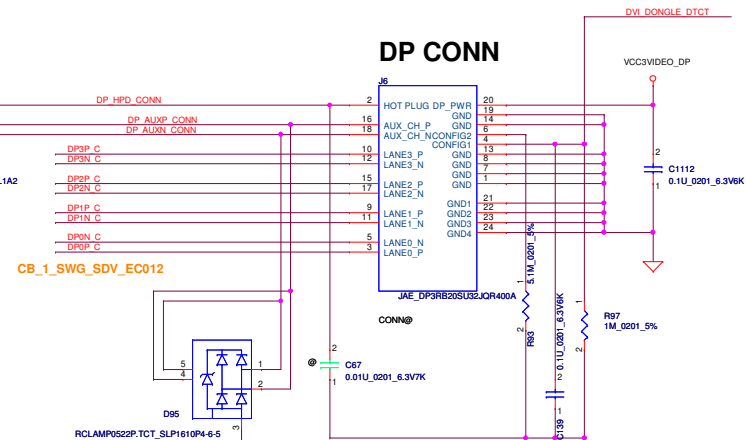
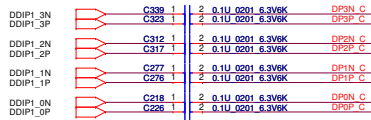
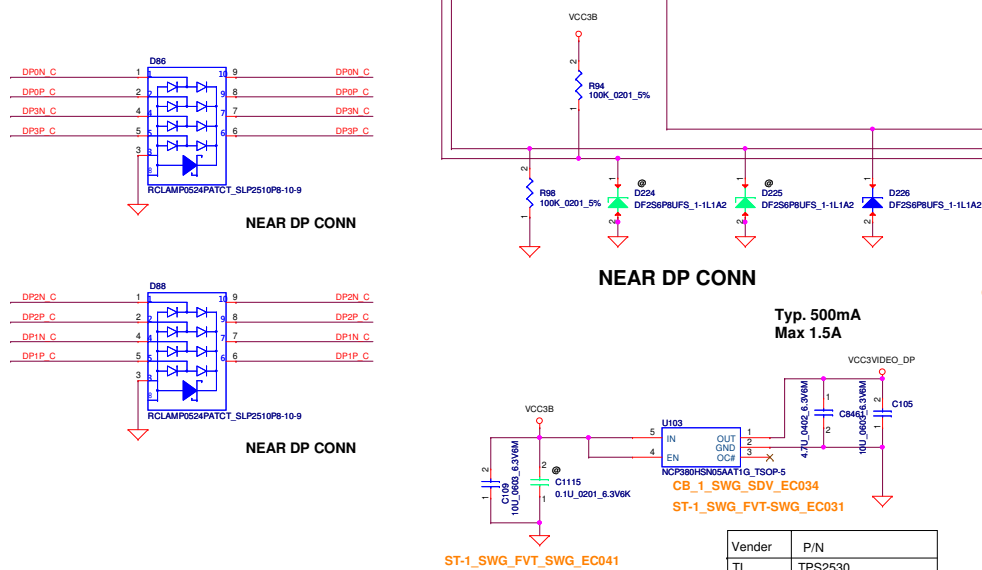
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2012/06/21		2012/06/21						
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						<small>Date:</small>	<small>Sheet</small>	<small>of</small>
						<small>Tuesday, July 30, 2013</small>	<small>39</small>	<small>100</small>

0.1





Vender	P/N
NXP	CBT3257ABQ
On-semi	74FST3257MNTWG




Vender	P/N
TI	TPS2530
On-semi	NCP380HSN05AAT1G

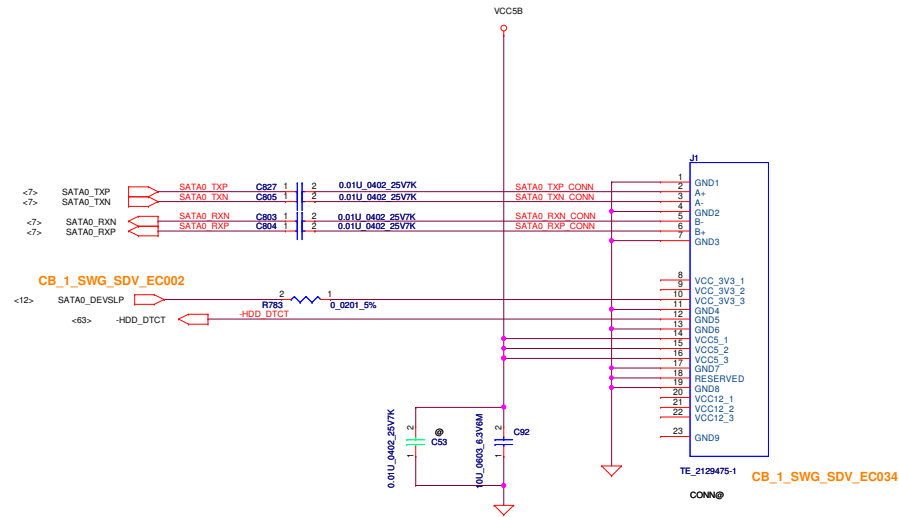
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Issued Date	2012/06/21	Deciphered Date	2012/06/21

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Title DISPLAY PORT CONNECTOR			
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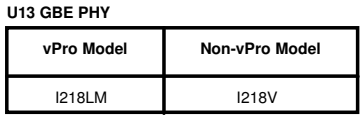
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		Date:		Tuesday, July 30, 2013		Sheet 42 of 100




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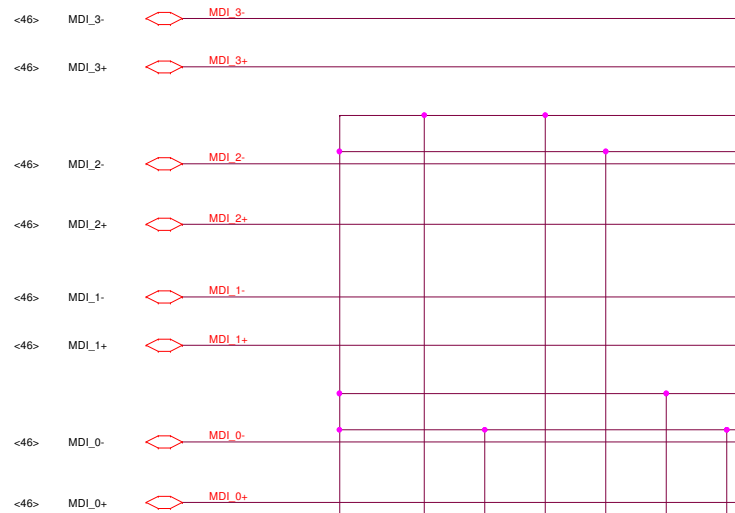
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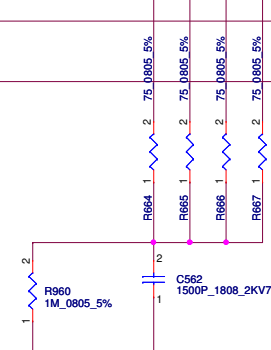
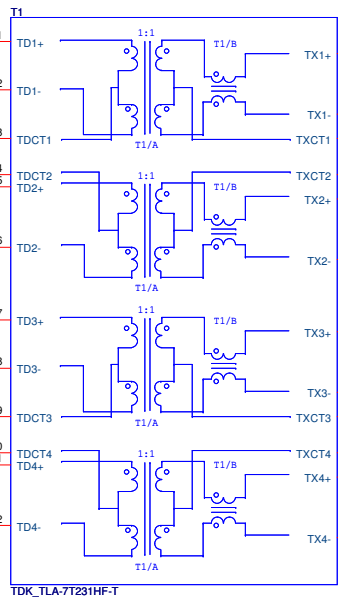
THE WIDTH OF THESE TRACE SHOULD BE WIDER THAN 35MIL TO PREVENT VOLTAGE DROP.

C303 SHOULD BE PLACED AS CLOSE TO MAGNETICS AS POSSIBLE.

ESD REASON

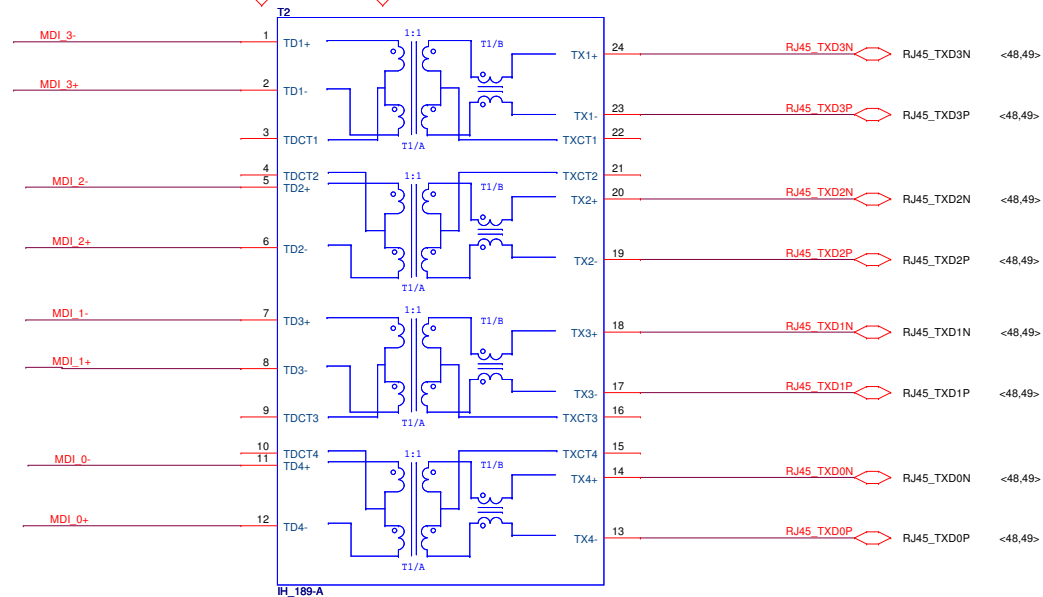
Vendor	P/N
TDK	TLA-7T231HF-T
Timag	IH-115-F
Bothand	NA69LF

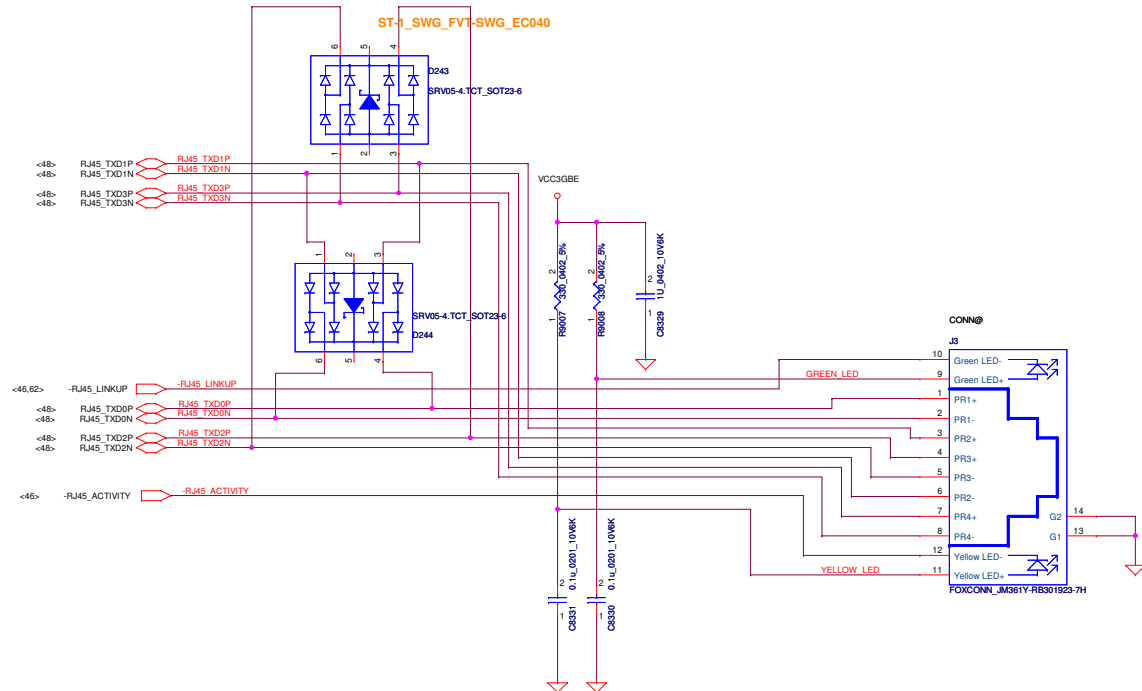
ST-1_SWG_FVT-SWG_EC017
ST-1_SWG_FVT-SWG_EC033



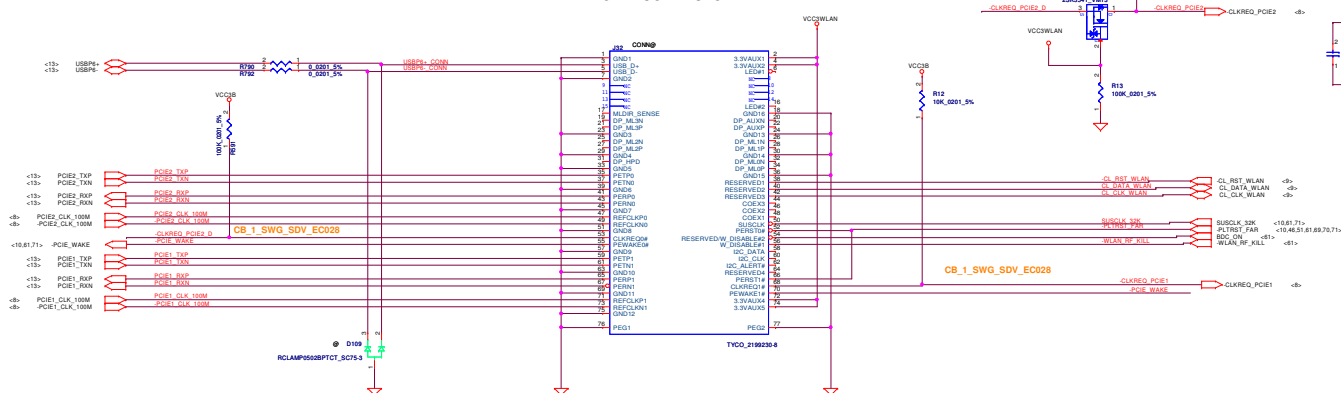
PATTERN MUST BE SHORT AND WIDE.

HIGH VOLTAGE 1500PF CAP IS OPTIONAL

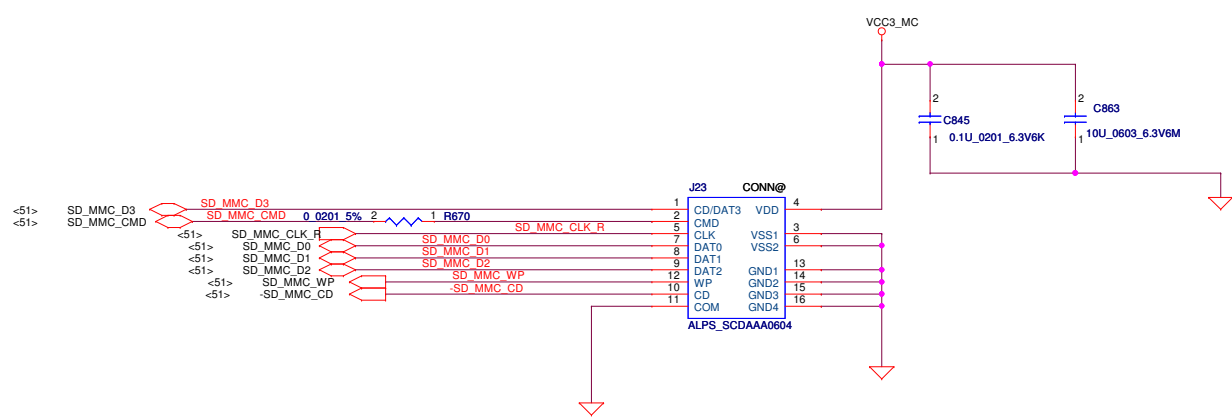




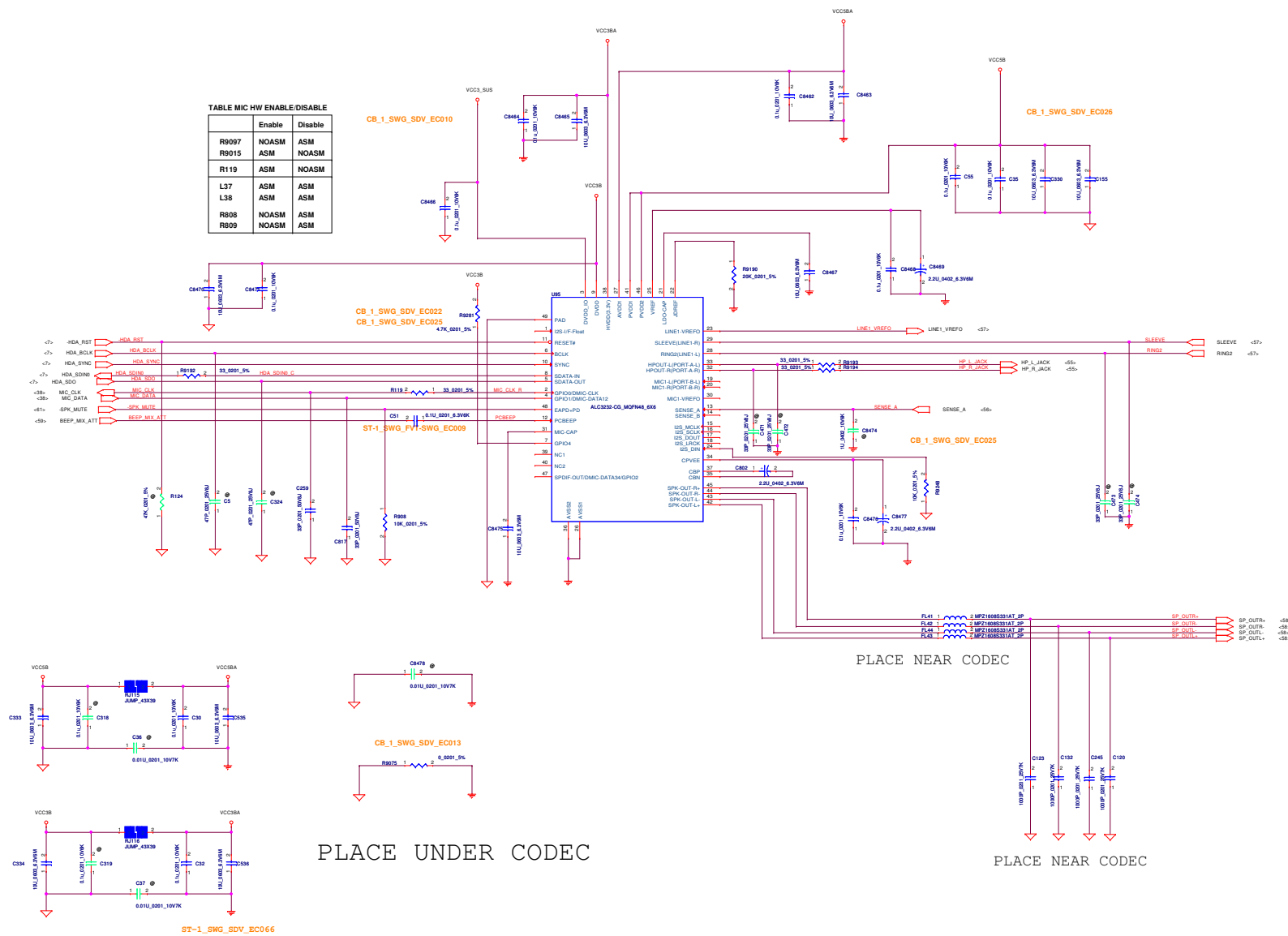
3.2H CONNECTOR

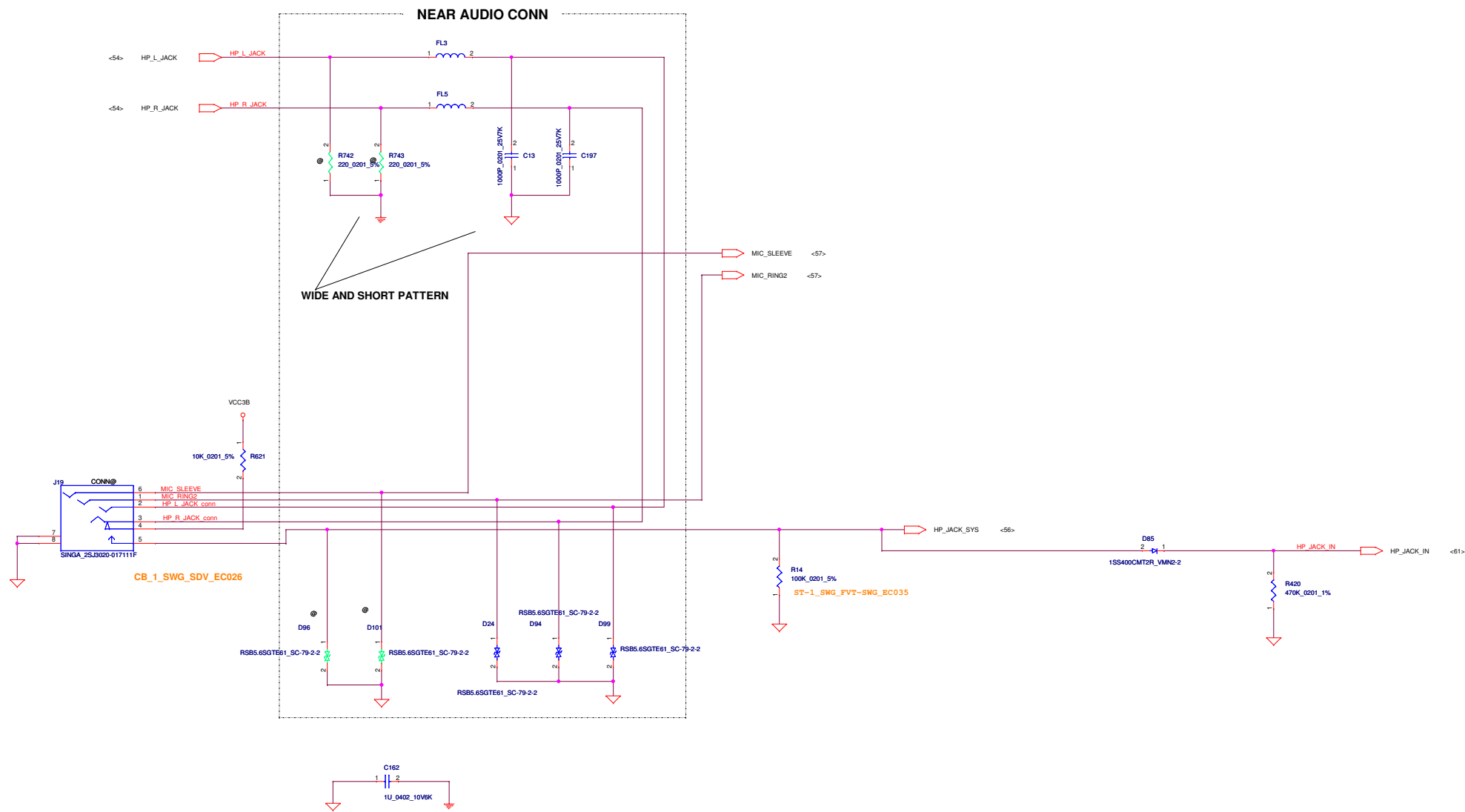


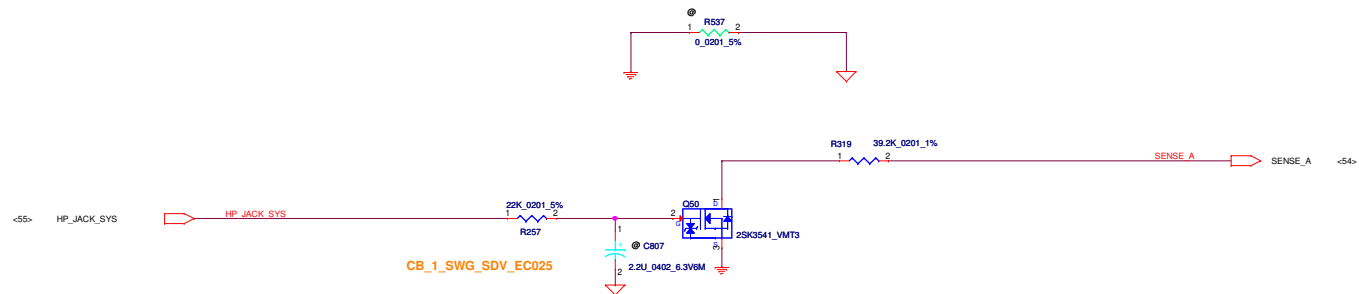
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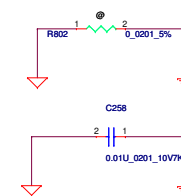
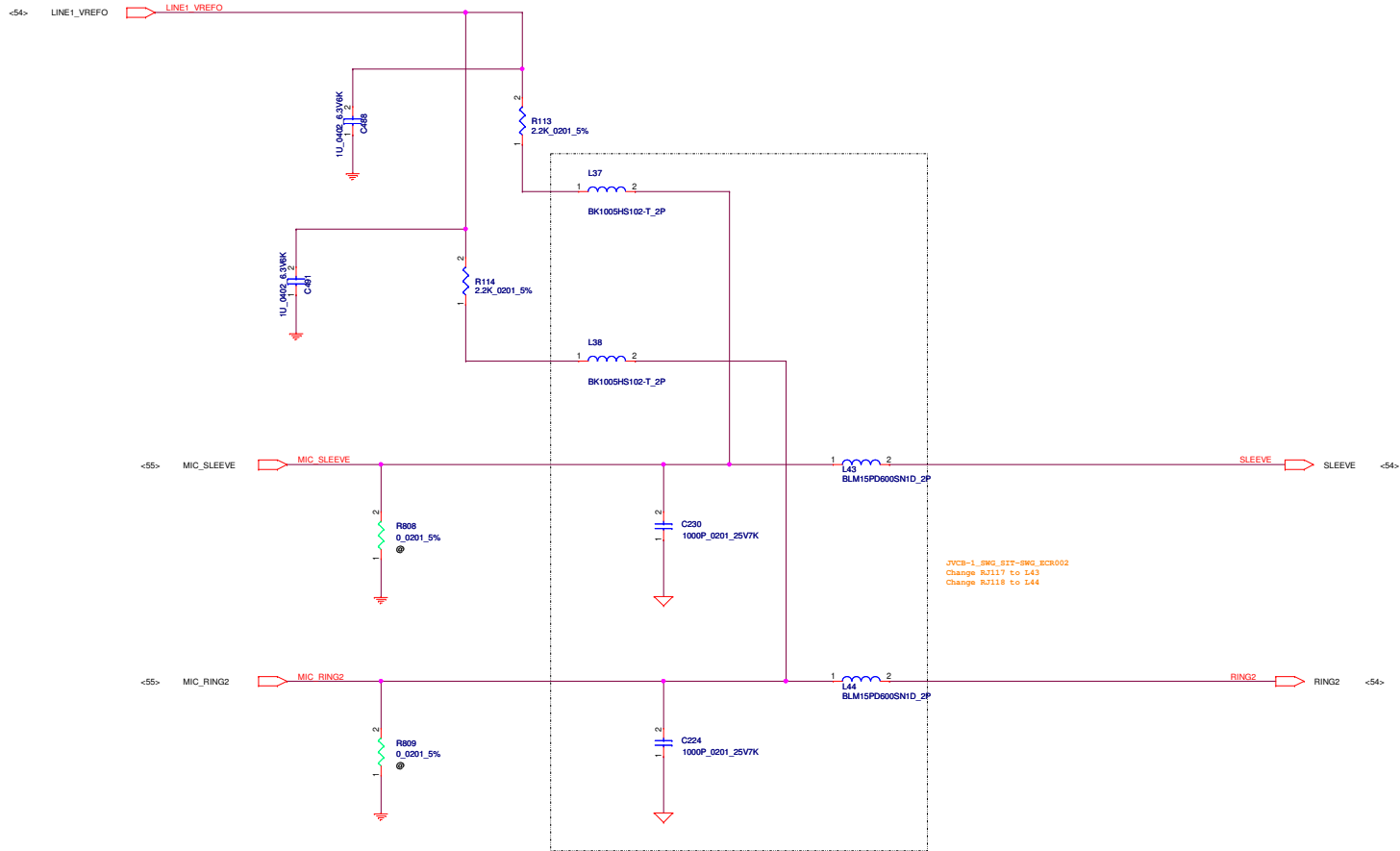


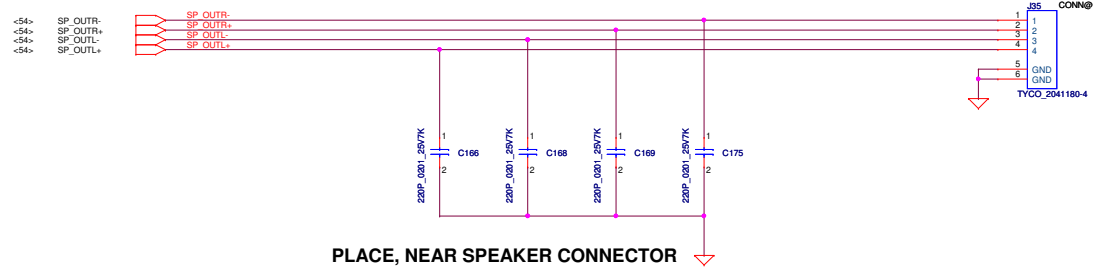
	Enable	Disable
R9097	NOASM	ASM
R9015	ASM	NOASM
R119	ASM	NOASM
L37	ASM	ASM
L38	ASM	ASM
R808	NOASM	ASM
R809	NOASM	ASM

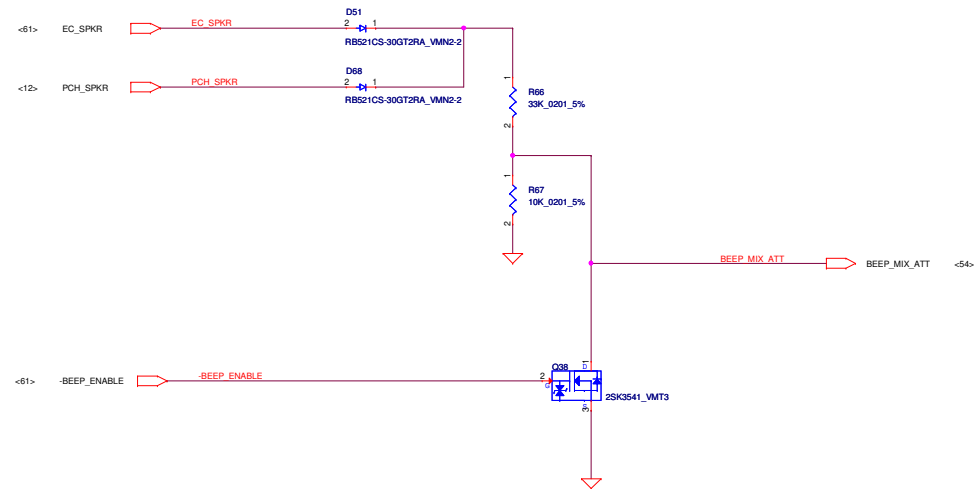







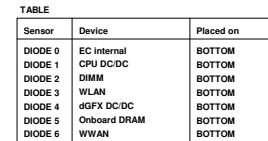


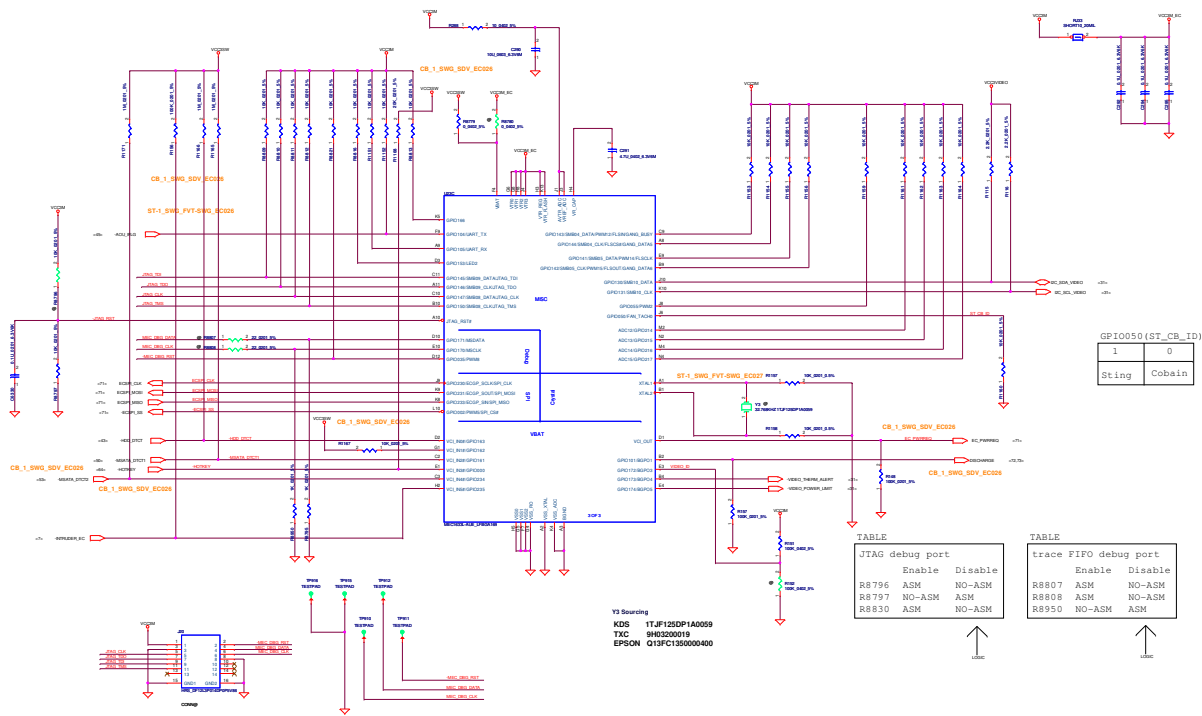




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GPIO50(ST_CB_ID)

1	0
Sting	Cobain

TABLE

JTAG debug port

	Enable	Disable
R8796	ASM	NO-ASM
R8797	NO-ASM	ASM
R8830	ASM	NO-ASM

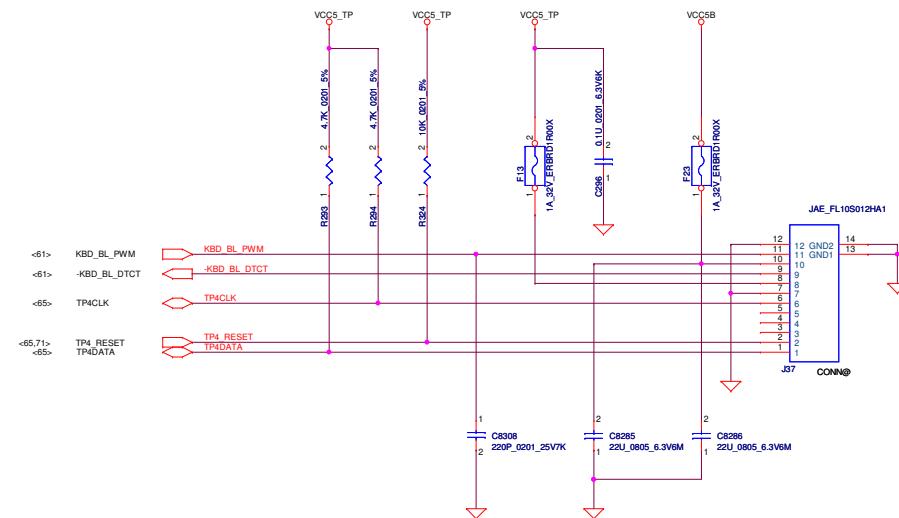
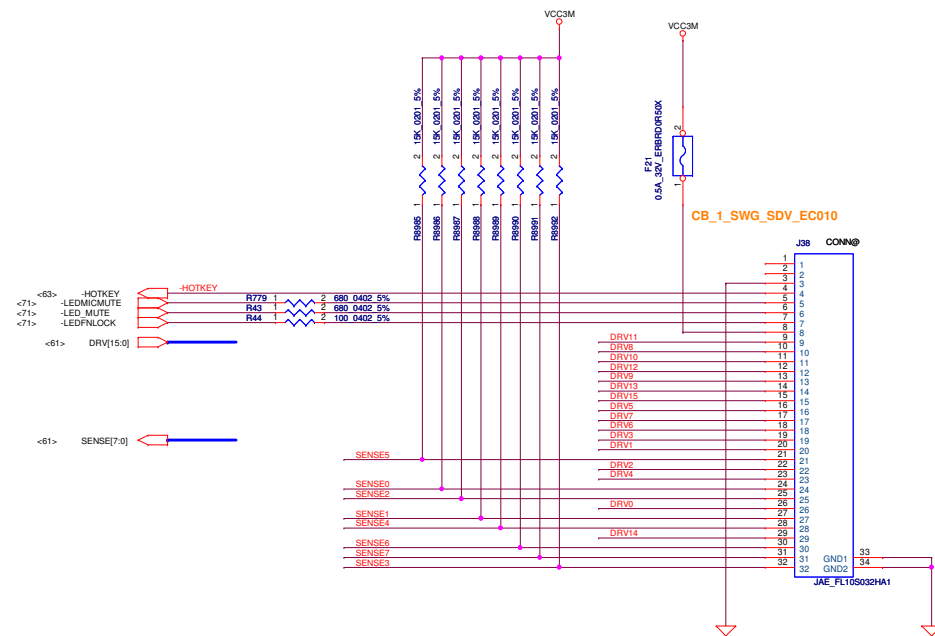
↑
LDR

TABLE


trace FIFO debug port

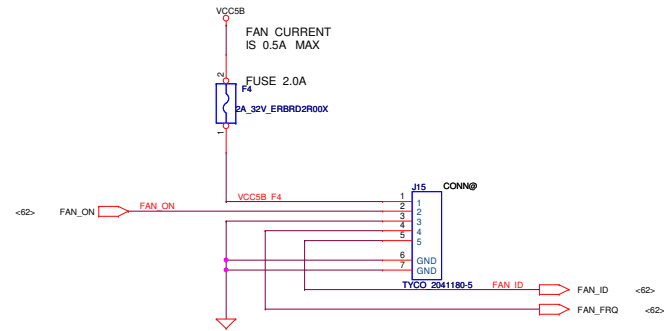
	Enable	Disable
R8807	ASM	NO-ASM
R8808	ASM	NO-ASM
R8950	NO-ASM	ASM

↑
LDR



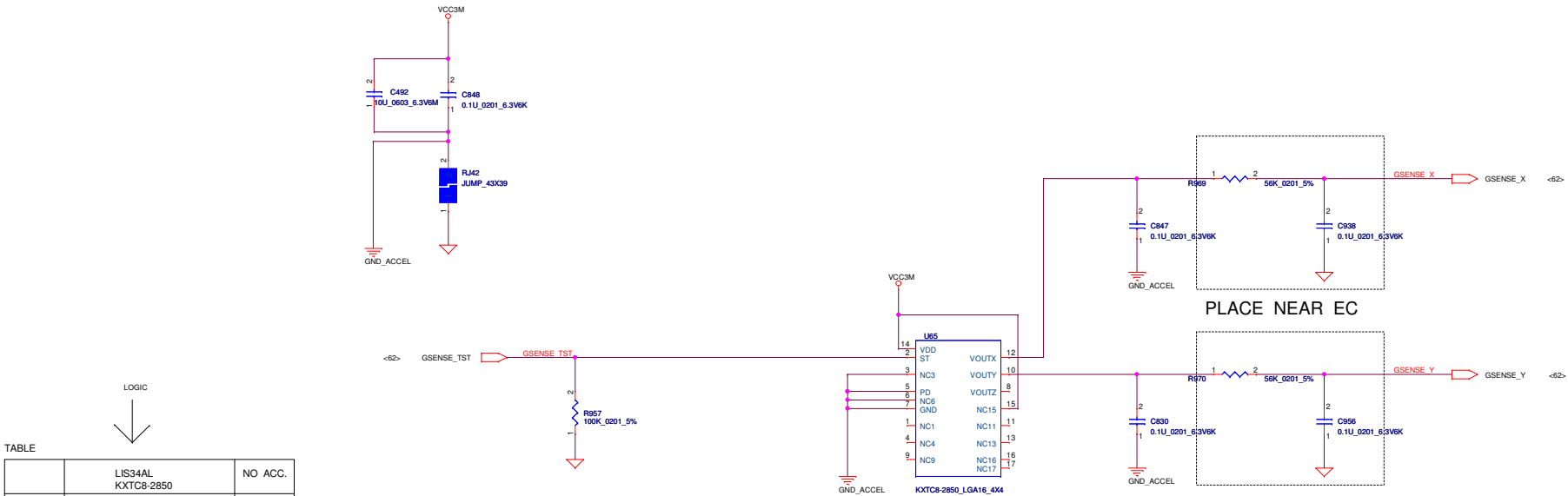
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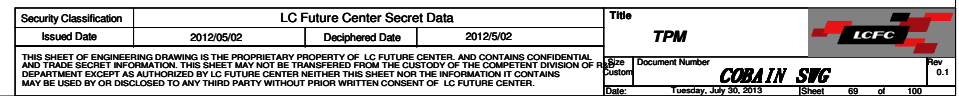
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						0.1	CORAIN SVG	Tuesday, July 30, 2013	66		



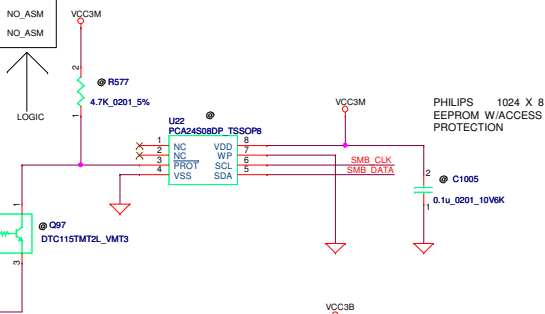
TABLE

	LIS34AL KXTC8-2850	NO ACC.
R401 R957	NO_ASM ASM	ASM ASM
U65	ASM	NO_ASM
Q105	ASM	NO_ASM
R885 C829 C969	10-OHM ASM ASM	NO_ASM NO_ASM NO_ASM
C830 C847	ASM ASM	NO_ASM NO_ASM
R969 C938 R970 C956	56K ASM 56K ASM	NO_ASM NO_ASM NO_ASM NO_ASM
C704 R344 C703	NO_ASM NO_ASM NO_ASM	NO_ASM NO_ASM NO_ASM
R125	ASM	ASM





EEPROM	U22	U23
U22	ASM	NO_ASM
C1005	ASM	NO_ASM
R577	ASM	NO_ASM
Q97	ASM	NO_ASM

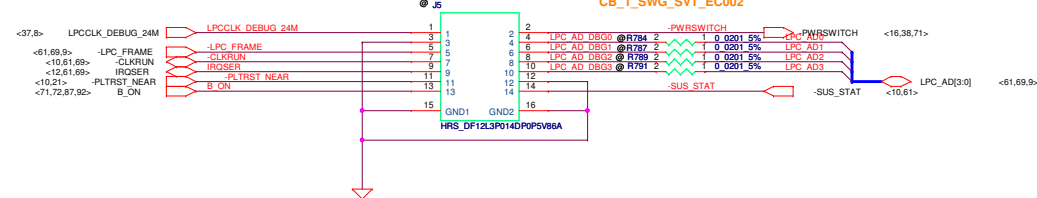


ST-1_SWG_SDV_EC132

REF DES	ENABLE	DISABLE
J5	ASM	NO_ASM
R220	ASM	NO_ASM

LOGIC

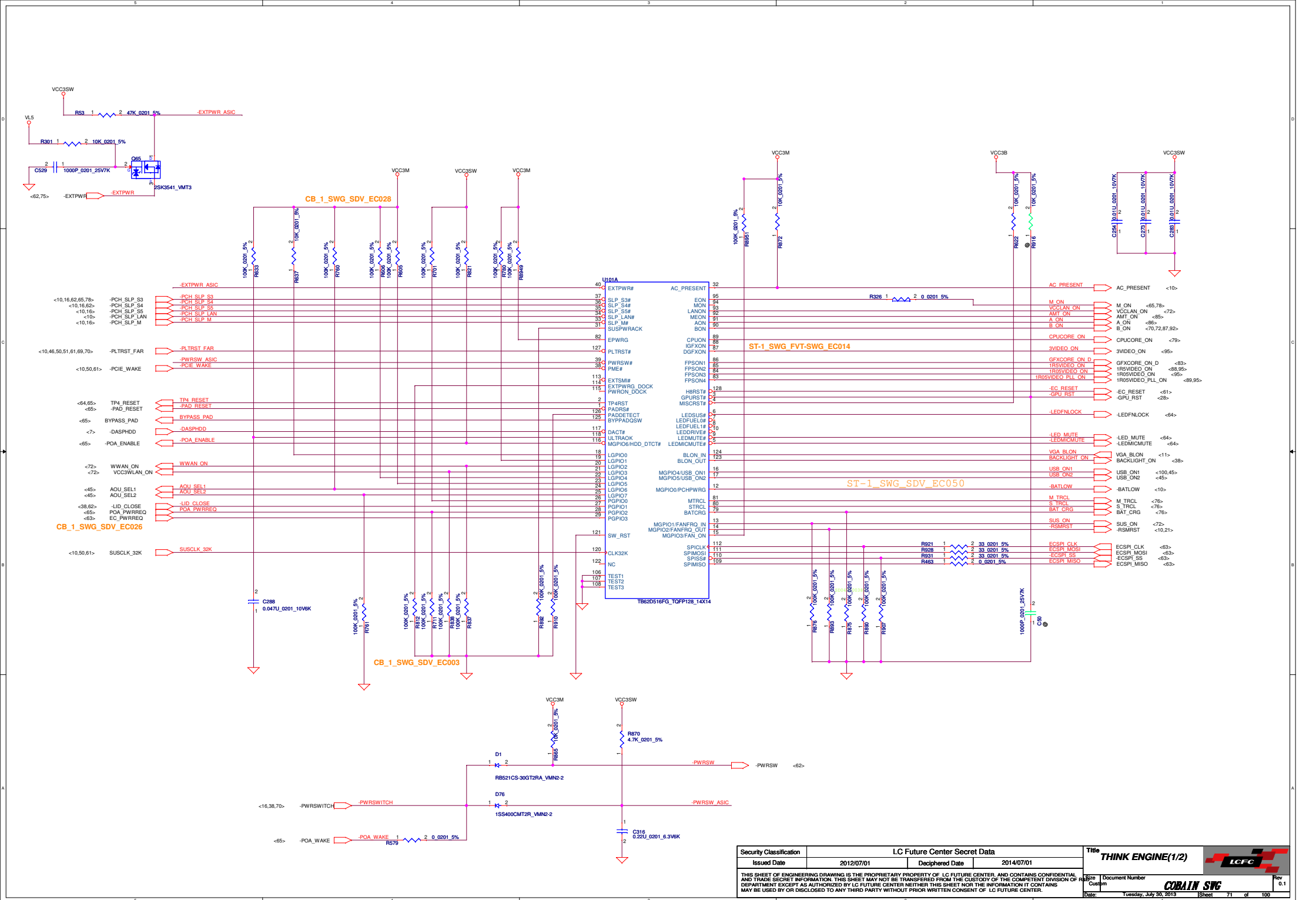
CB_1_SWG_SDV_EC022



CB_1_SWG_SDV_EC028
CB_1_SWG_SVT_EC002

EEPROM	U22	U23
U21	ASM	NO_ASM
U31	ASM	NO_ASM
C25	ASM	NO_ASM
R291	ASM	NO_ASM
Q84	ASM	NO_ASM
R8941	NO_ASM	ASM
R8940	NO_ASM	ASM
R30	ASM	NO_ASM
R45	ASM	NO_ASM

LOGIC



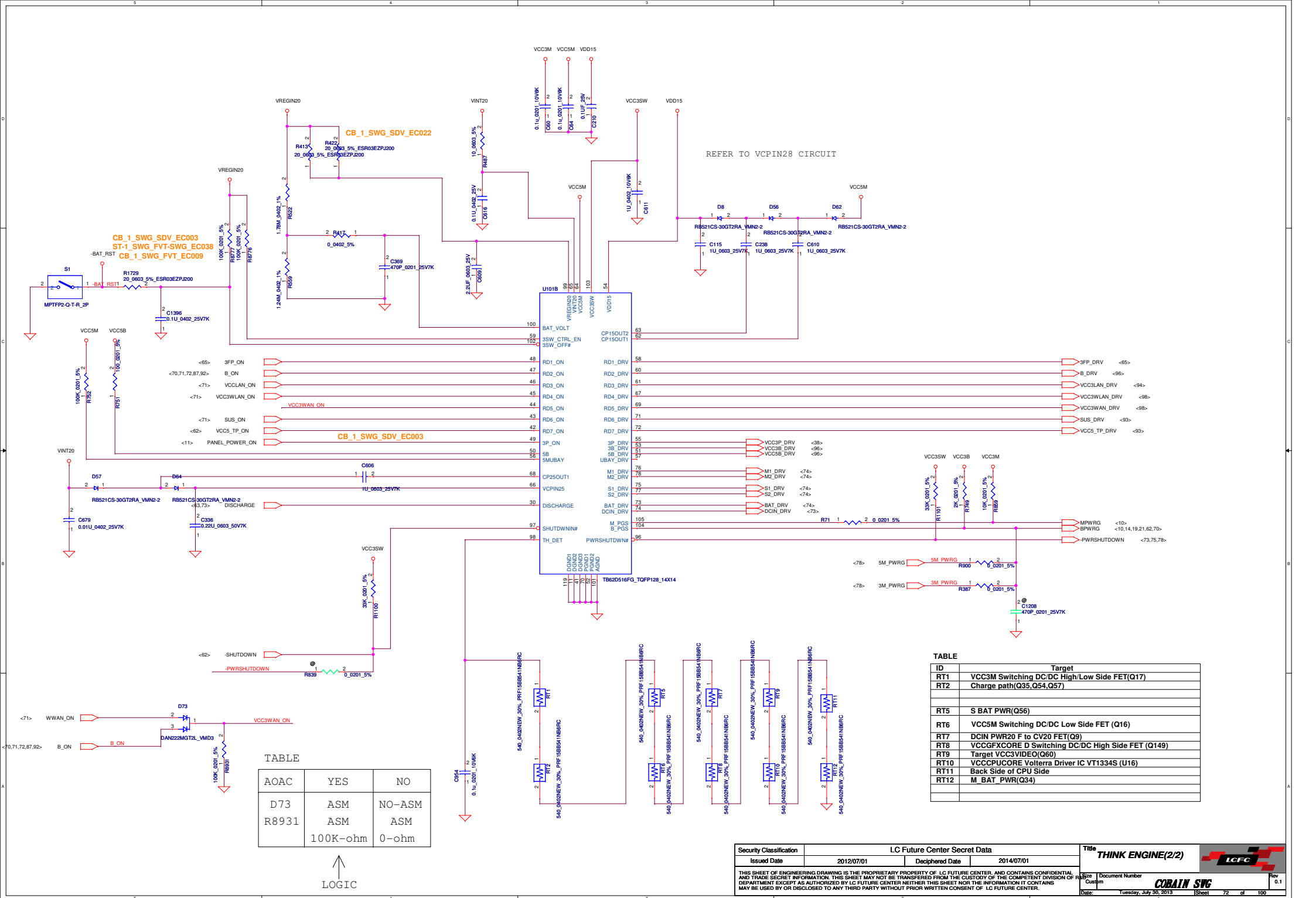
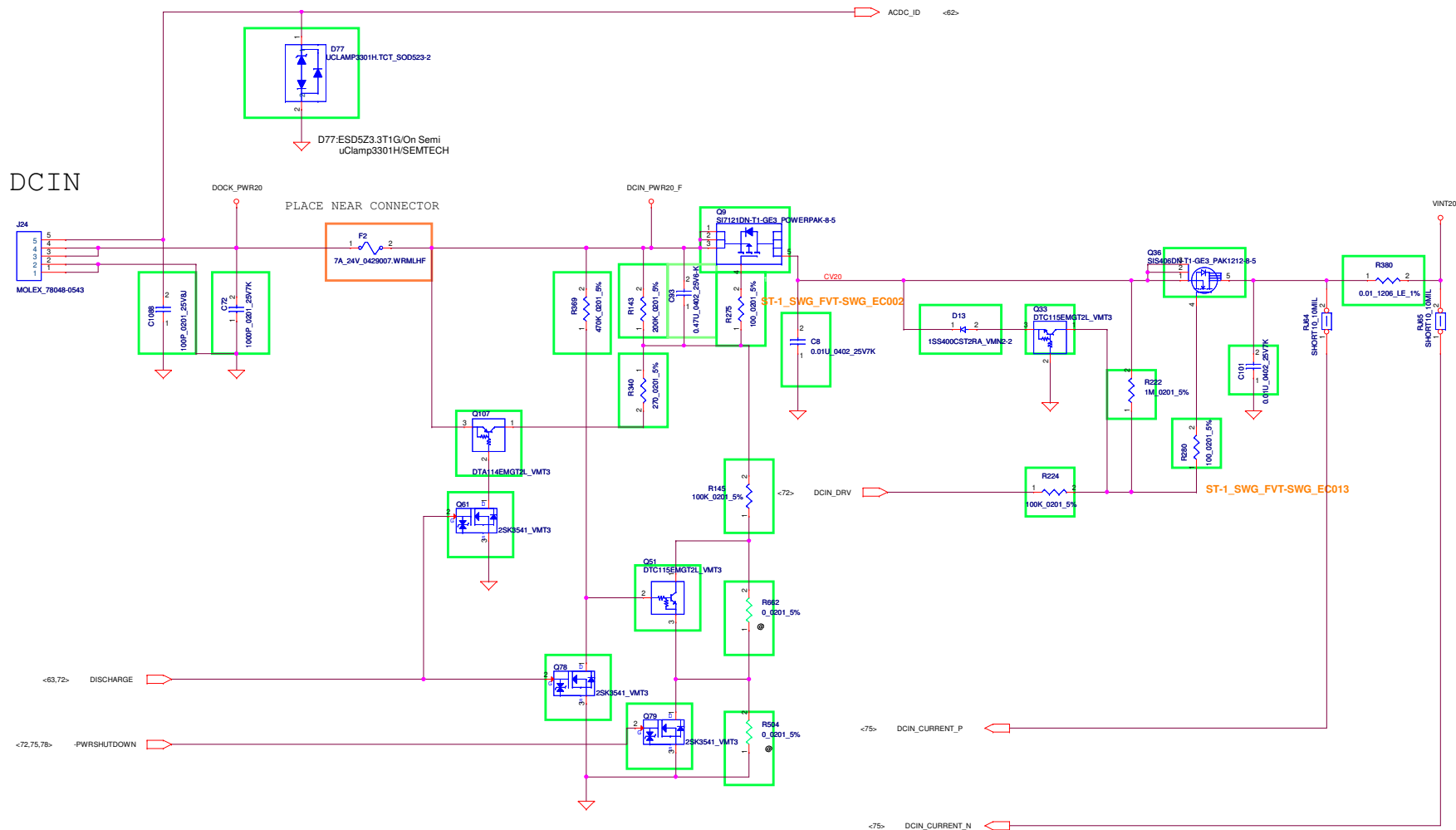


TABLE		
AOAC	YES	NO
D73	ASM	NO-ASM
R8931	ASM	ASM
	100K-ohm	0-ohm

TABLE	
ID	Target
RT1	VCC3M Switching DC/DC High/Low Side FET(Q17)
RT2	Charge path(Q35,Q54,Q57)
RT5	S BAT PWR(Q56)
RT6	VCC5M Switching DC/DC Low Side FET (Q16)
RT7	DCIN PWR20 F to CV20 FET(Q9)
RT8	VCCGFCORE D Switching DC/DC High Side FET (Q149)
RT9	Target VCC3VIDEO(Q60)
RT10	VCCCPUCORE Valtterra Driver IC VT1334S (U16)
RT11	Back Side of CPU Side
RT12	M BAT PWR(Q34)

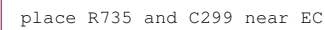
DCIN





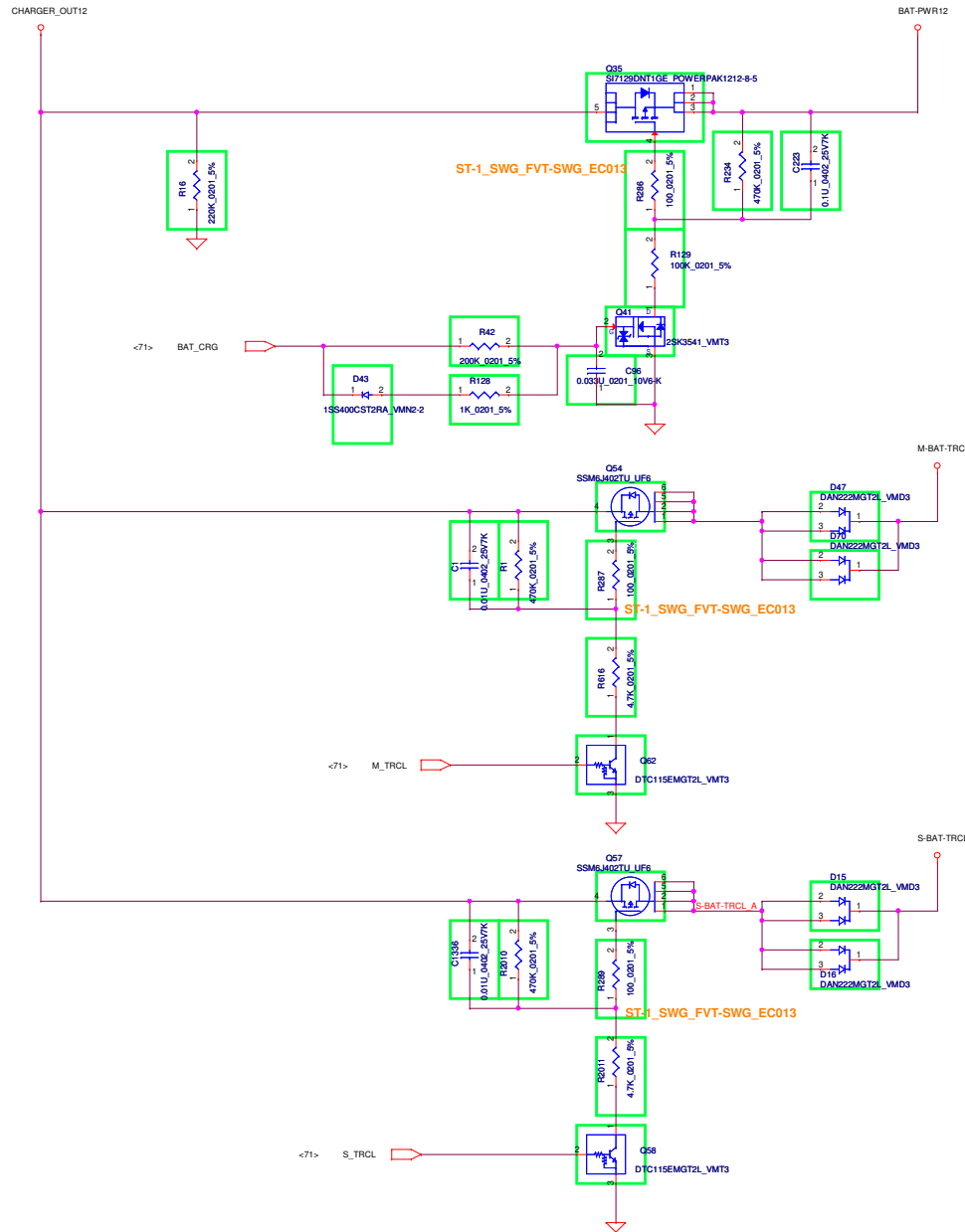
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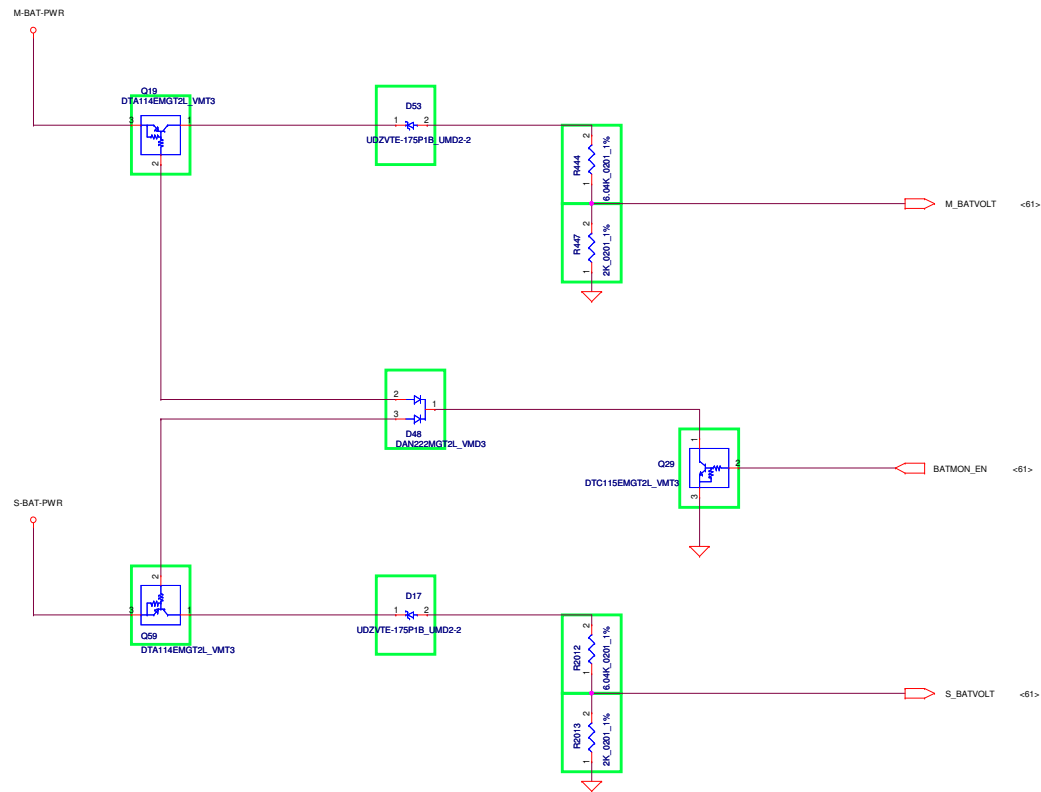
PEAK SHIFT	YES	NO
R662	NO-ASM	ASM
R369	ASM	NO-ASM
Q78	ASM	NO-ASM
Q51	ASM	NO-ASM

↑
LOGIC



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				Document Number	
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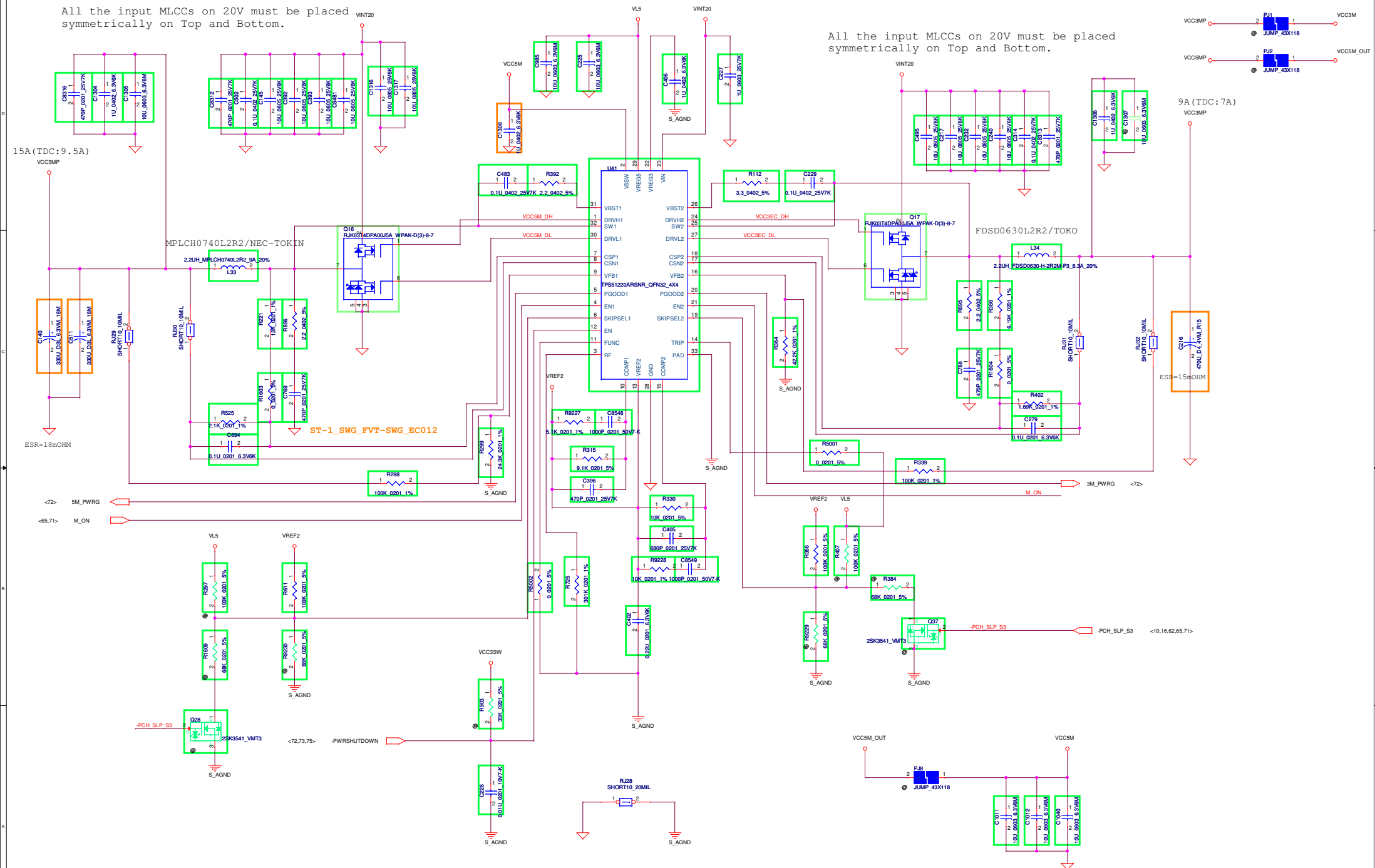





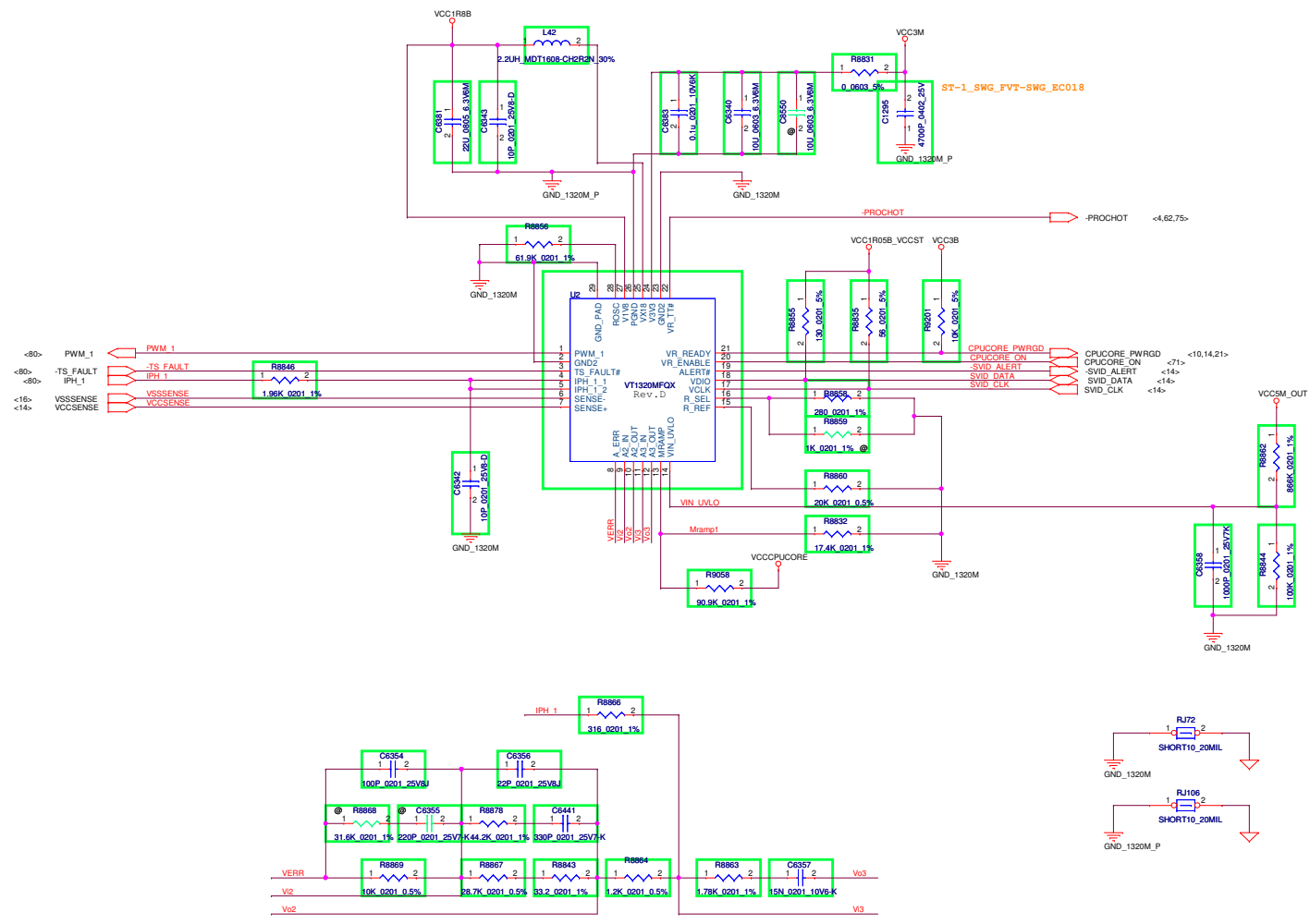
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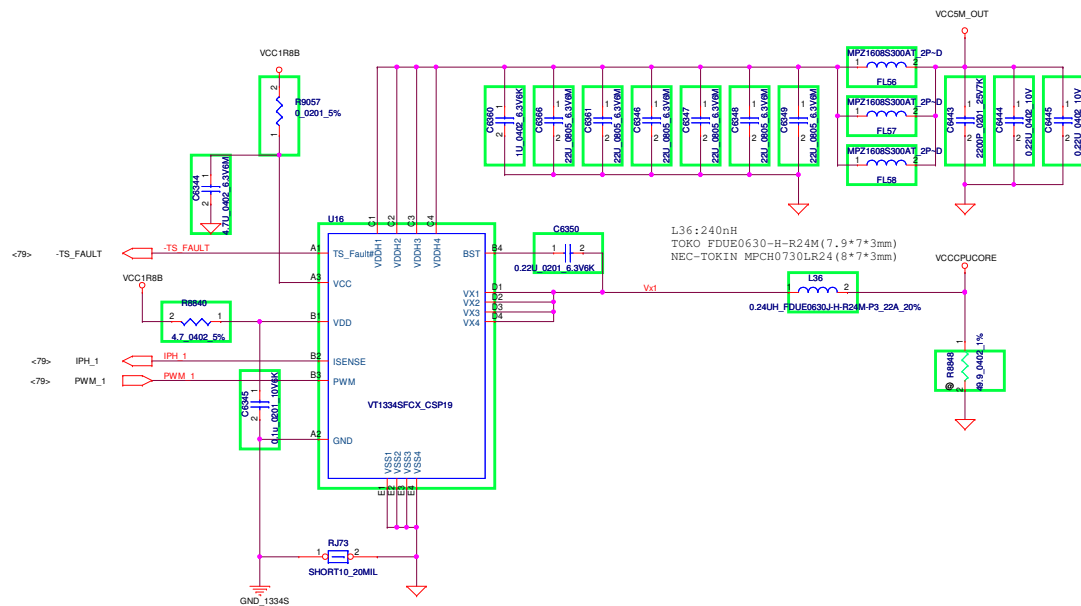
Cobain SWG

All the input MLCCs on 20V must be placed symmetrically on Top and Bottom.




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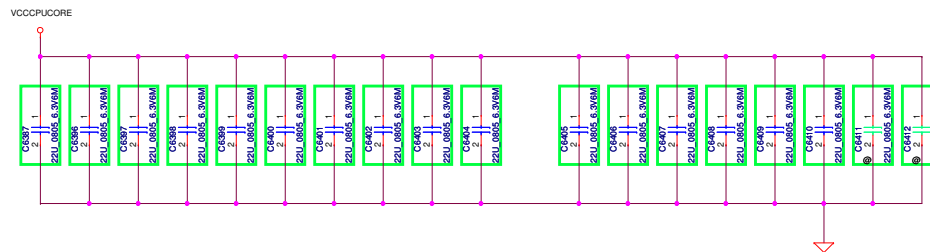
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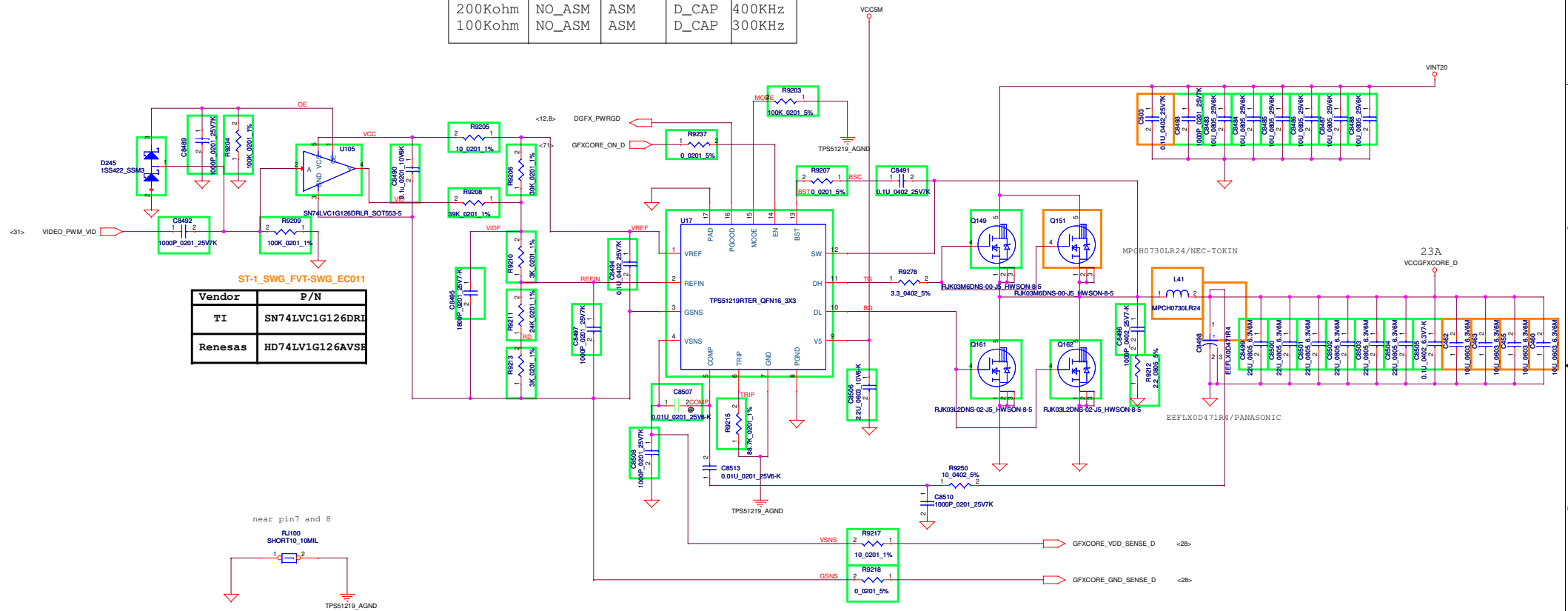
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16pcs 22uF for VCCCPUCORE of 25W ULT CPU
(14pcs 22uF for VCCCPUCORE of 15W ULT CPU)


R9203	C8507	C8513	mode	sw freq
1Kohm	ASM	NO_ASM	D_CAP2	500KHz
200Kohm	NO_ASM	ASM	D_CAP	400KHz
100Kohm	NO_ASM	ASM	D_CAP	300KHz

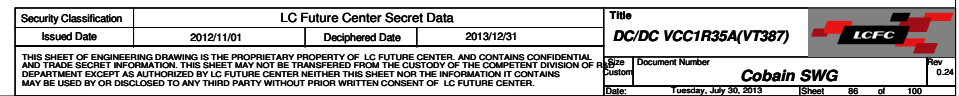


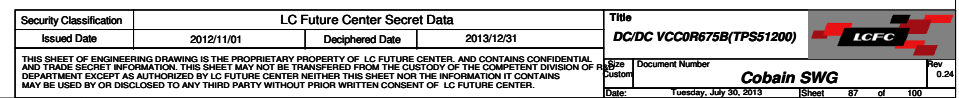
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Issued Date	2012/11/01	Deciphered Date	2013/12/31	DC/DC VCCGFCXCORE_0(TPSS51219) 		
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				Date:	Tuesday, July 30, 2013	Sheet

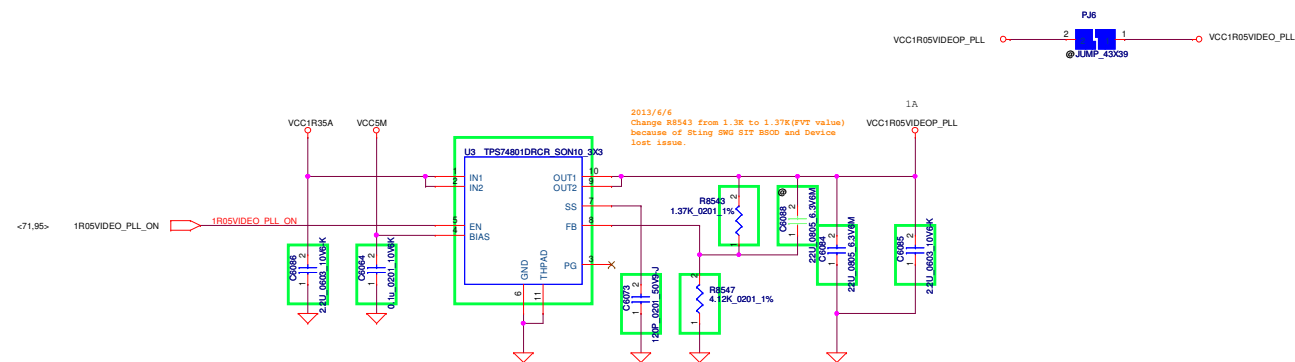
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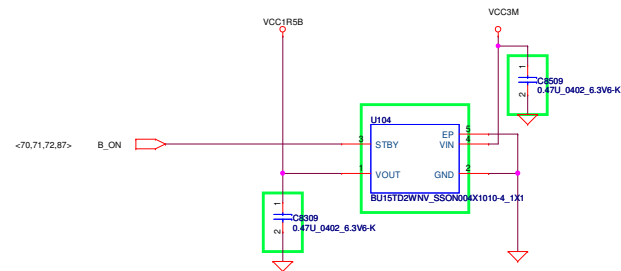
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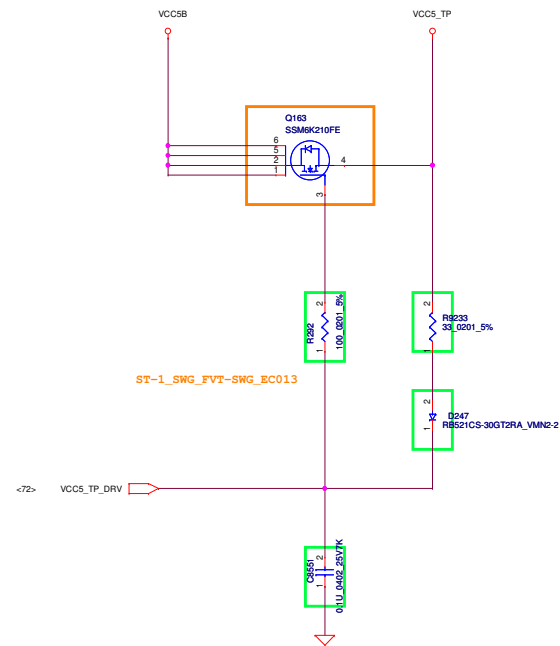
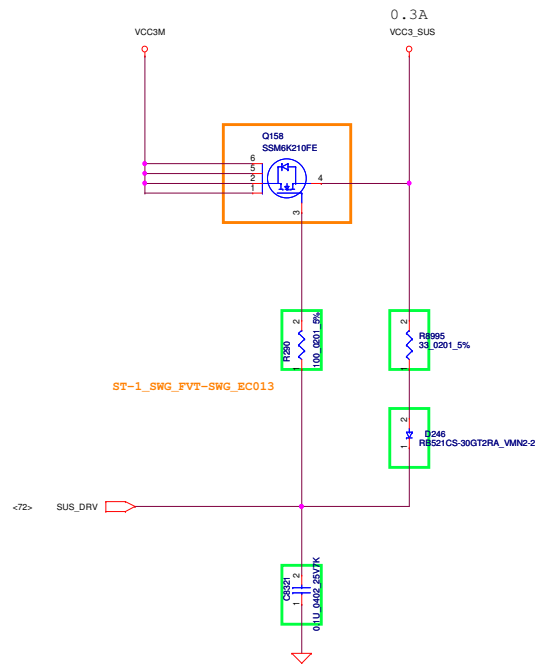
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				0.24	1876
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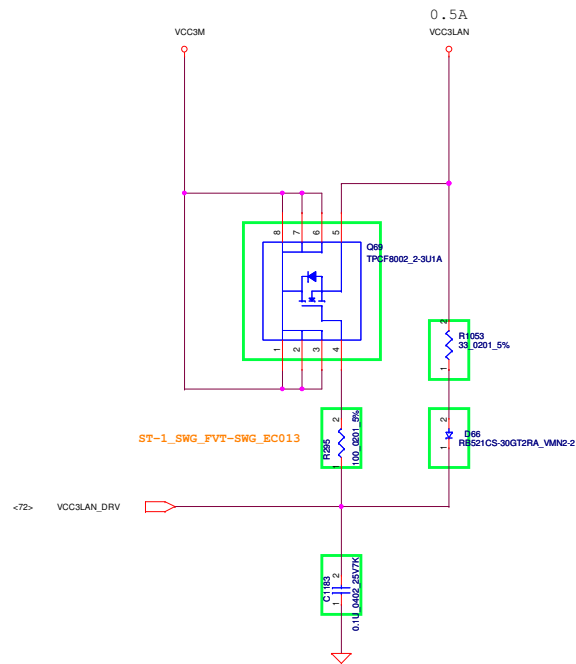

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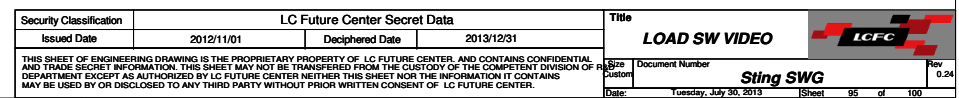
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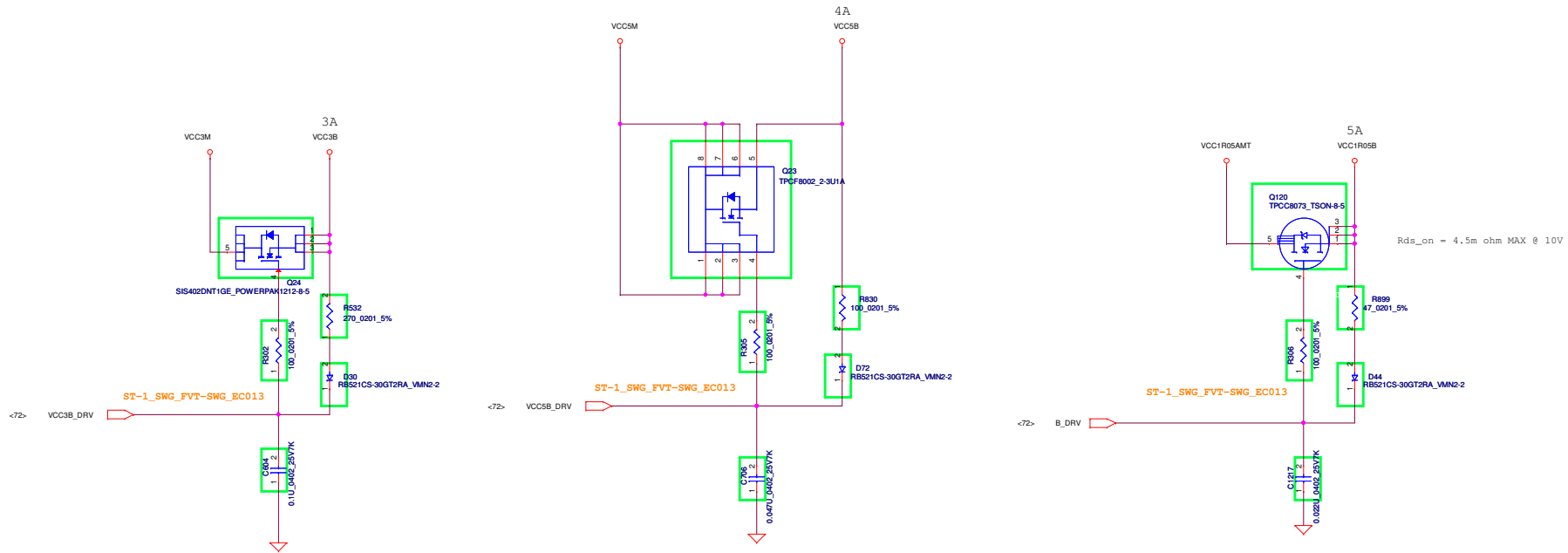


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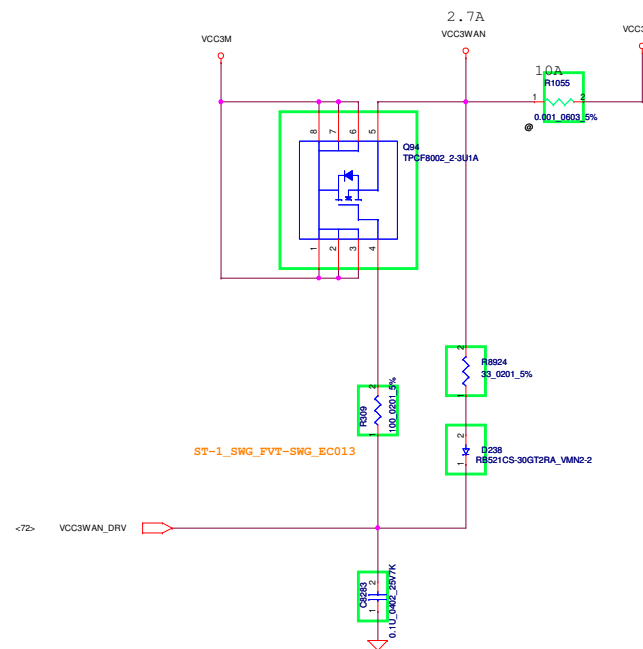
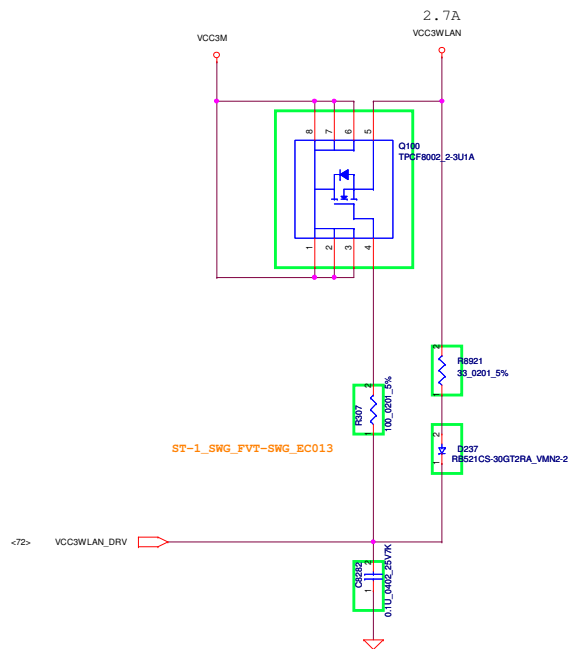
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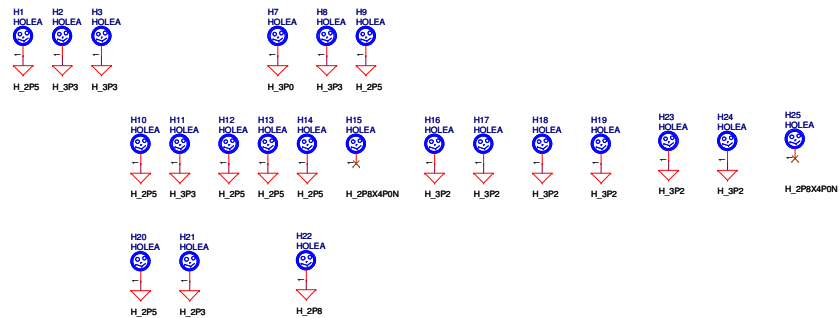
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TABLE

AOAC	YES	NO
R1055	NO-ASM	ASM
Q94	ASM	NO-ASM
R8924	ASM	NO-ASM
R8926	ASM	NO-ASM
C8283	ASM	NO-ASM
D238	ASM	NO-ASM

↑
LOGIC



FID
Board Area

FID
Component Area



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COBAIN SWG

